



**1A LOW DROPOUT POSITIVE  
FIXED 1.8V REGULATOR**

**FEATURES**

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 2% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, SOT-89, TO-263 and 8-Pin SOIC Surface-Mount Packages

**DESCRIPTION**

The APU1117-18 is a low dropout three-terminal fixed output regulator with minimum of 1A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications as well as generating clock supply for PC applications. The APU1117-18 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated with 3.8V input supply. The APU1117-18 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

**APPLICATIONS**

- Low Voltage IC Supply Applications
- PC Clock Supply Voltage

**TYPICAL APPLICATION**

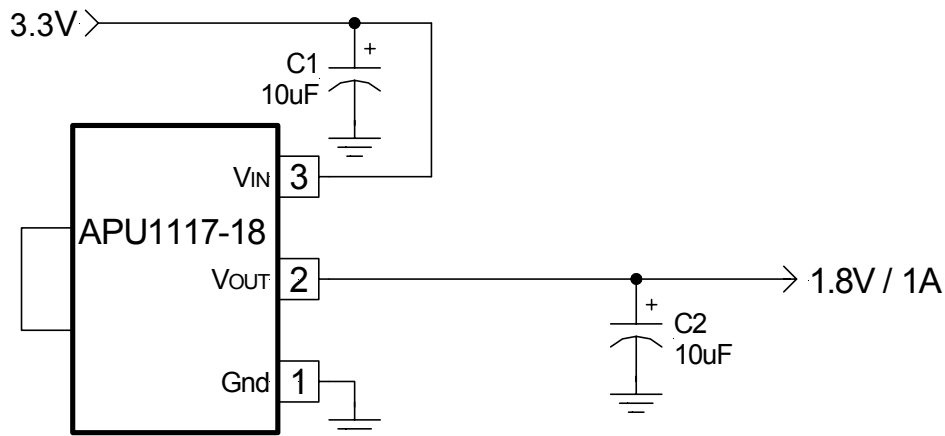


Figure 1 - Typical application of APU1117-18 in a 3.3V to 1.8V regulator.

**PACKAGE ORDER INFORMATION**

Leadfree Part

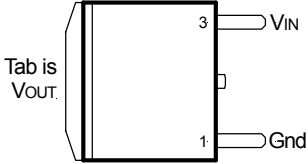
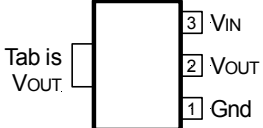
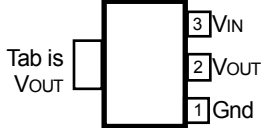
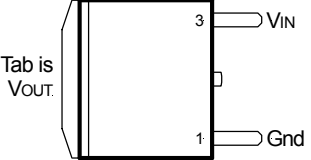
T <sub>J</sub> (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC SOT-223	3-PIN PLASTIC SOT-89	2-PIN PLASTIC TO-263
0 To 125	APU1117H-18	APU1117K-18	APU1117G-18	APU1117S-18



**ABSOLUTE MAXIMUM RATINGS**

Input Voltage (V <sub>IN</sub> ) .....	7V
Power Dissipation .....	Internally Limited
Storage Temperature Range .....	-65°C To 150°C
Operating Junction Temperature Range .....	0°C To 150°C

**PACKAGE INFORMATION**

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC SOT-223 (K)	3-PIN PLASTIC SOT-89 (G)	2-PIN PLASTIC TO-263 (S)
 <p>Tab is V<sub>OUT</sub>.</p> <p><math>\theta_{JA}=70^{\circ}\text{C/W}</math> for 0.5" Sq pad</p>	 <p>Tab is V<sub>OUT</sub>.</p> <p><math>\theta_{JA}=90^{\circ}\text{C/W}</math> for 0.4" Sq pad</p>	 <p>Tab is V<sub>OUT</sub>.</p> <p><math>\theta_{JA}=100^{\circ}\text{C/W}</math> for Min" Sq pad</p>	 <p>Tab is V<sub>OUT</sub>.</p> <p><math>\theta_{JA}=35^{\circ}\text{C/W}</math> for 1" Sq pad</p>

**ELECTRICAL SPECIFICATIONS**

Unless otherwise specified, these specifications apply over C<sub>IN</sub>=1μF, V<sub>IN</sub>=5V, C<sub>OUT</sub>=10μF, and T<sub>J</sub>=0 to 125°C. Typical values refer to T<sub>J</sub>=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V <sub>o</sub>	I <sub>o</sub> =10mA, T <sub>J</sub> =25°C	1.764	1.800	1.836	V
Line Regulation		I <sub>o</sub> =10mA, 4.75V<V <sub>IN</sub> <7V			7	mV
Load Regulation (Note 1)		10mA<I <sub>o</sub> <1A			1	%
Dropout Voltage (Note 2)		I <sub>o</sub> =1A			1.3	V
Current Limit		ΔV <sub>o</sub> =100mV	1.1			A
Thermal Regulation		30ms Pulse, I <sub>o</sub> =1A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, C <sub>o</sub> =25μF Tantalum, I <sub>o</sub> =0.5A	60	70		dB
Temperature Stability		I <sub>o</sub> =10mA		0.5		%
Long Term Stability		T <sub>J</sub> =125 °C, 1000Hrs		0.3	1	%
RMS Output Noise		T <sub>J</sub> =25°C, 10Hz<f<10KHz		0.003		%V <sub>o</sub>

**Note 1:** Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

**Note 2:** Dropout voltage is defined as the minimum differential voltage between V<sub>IN</sub> and V<sub>OUT</sub> required to maintain regulation at U<sub>T</sub>. It is measured when the output voltage drops 1% below its nominal value.



## PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	V <sub>OUT</sub>	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	V <sub>IN</sub>	Input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than V <sub>OUT</sub> in order for the device to regulate properly.

## BLOCK DIAGRAM

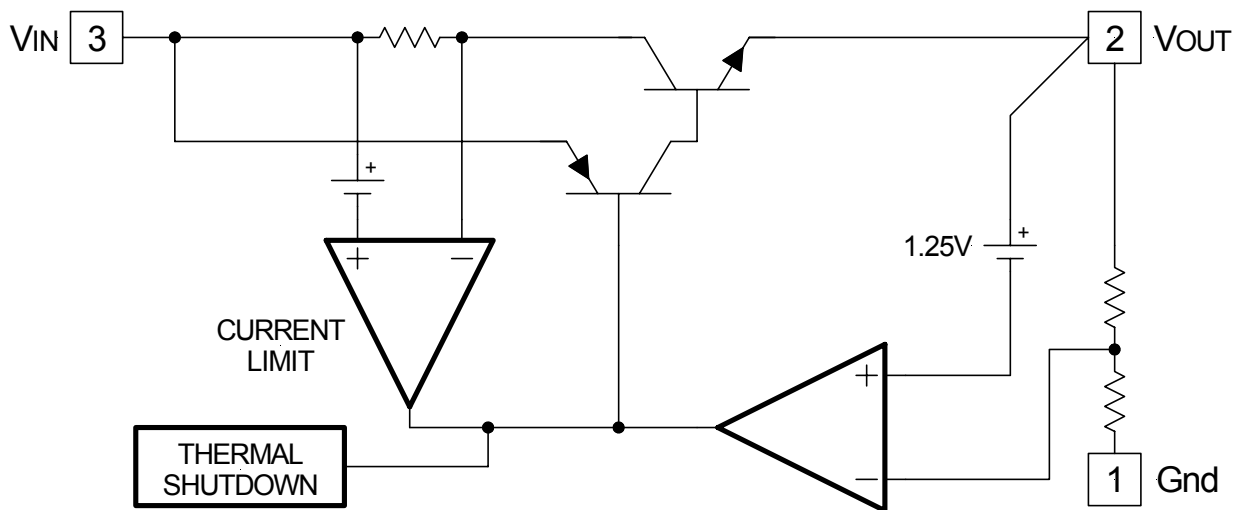


Figure 2 - Simplified block diagram of the APU1117-18.