OVER CURRENT PROTECTION IC WITH SHUNT REGULATOR

GENERAL DESCRIPTION

FP133 is a main rail current detection and over current protection IC. It is including a current shunt comparator and shutdown comparator with a precision shunt regulator like **FP431**.

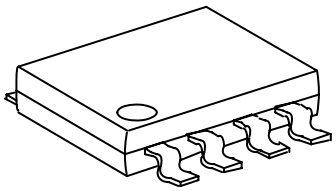
The current shunt comparator has the any gain adjustable function for rail current detection using three external resistors, and inter-connecting to a shutdown comparator for driving a protection circuit like a photo-coupler to shutdown the primary side PWM IC when over current is occurred.

And the voltage shunt regulator has a **2.5V** reference for switching power supply secondary output voltage feedback.

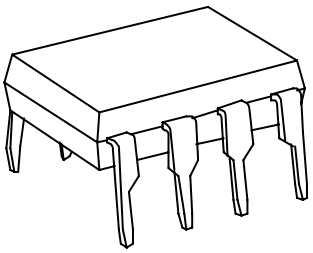
FP133 is used with a few external parts for O.C.P. and output voltage feedback function and good active point during wide temperature range in secondary main rail power supply of SPS or isolated fly-back DC-DC converter application field.

FEATURES

- Wide operating voltage range: +2.7V~ +30V
- Wide operating temperature range: -20℃~ +105℃
- Independent shunt and supply voltage
- Low input offset voltage
- Sense gain adjustable
- Built-in 1.25V comparator for O.C.P.
- Shunt regulator voltage: 2.5V (0.5%)
- FPO Output sink current capability up 40mA
- Package: PDIP8/SOP8



SOP8

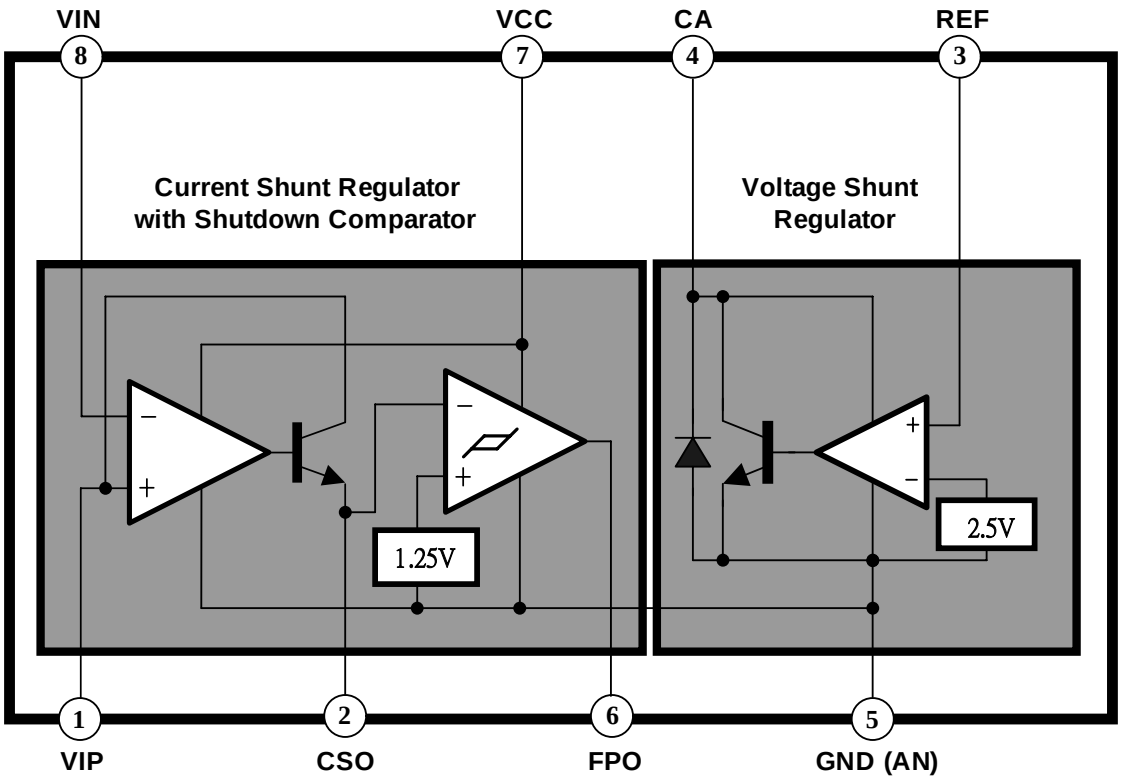


PDIP8

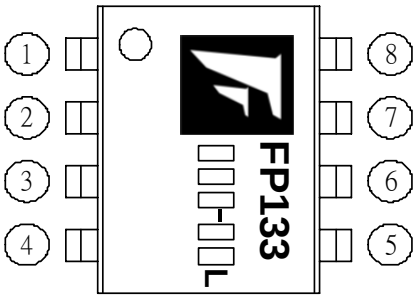
TYPICAL APPLICATION

- SPS
- AC Adaptor
- Isolated Fly-back DC-DC Converter

FUNCTIONAL BLOCK DIAGRAM



MARK VIEW



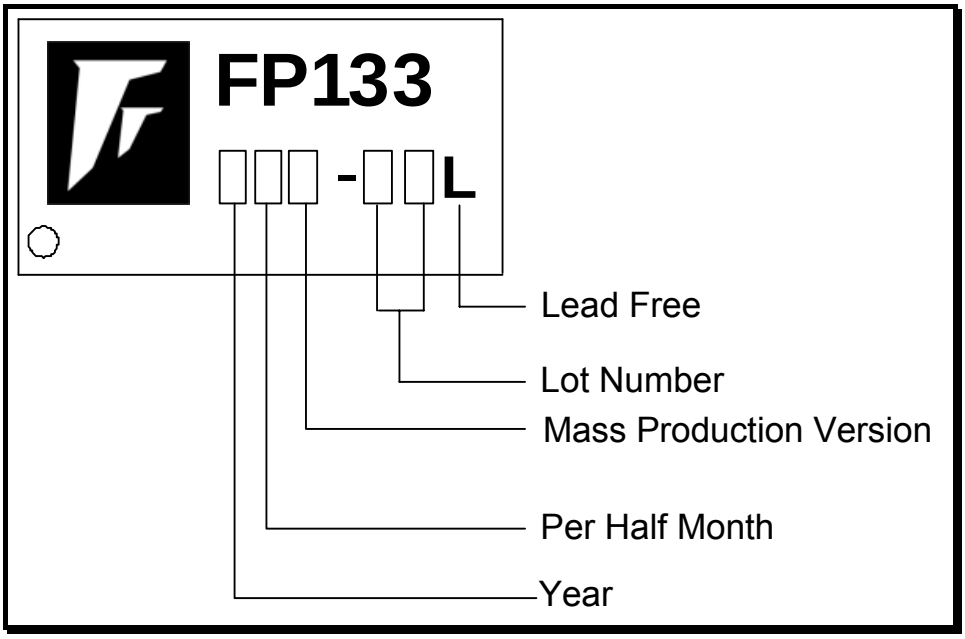
PIN DESCRIPTION

Name	No.	Status	Description
VIP	1	I	Positive Input of Current Shunt OPA
CSO	2	O/I	Output of Current Shunt OPA to Inverting of Shutdown Comparator
REF	3	I	2.5V Reference
CA	4	I	Voltage Shunt Cathode Input
GND	5	P	IC Ground
FPO	6	O	Shutdown Comparator Output (O.C.)
VCC	7	P	IC Power Supply
VIN	8	I	Negative Input of Current Shunt OPA

ORDER INFORMATION

Part Number	Operating Temperature	Package	Description
FP133P-LF	-20℃ ~ +105℃	PDIP8	Tube
FP133D-LF	-20℃ ~ +105℃	SOP8	Tube
FP133DR-LF	-20℃ ~ +105℃	SOP8	Tape & Reel

IC DATE CODE DISTINGUISH



FOR EXAMPLE:

January A (Front Half Month), B (Last Half Month)
February C, D
March E, F ----------And so on.

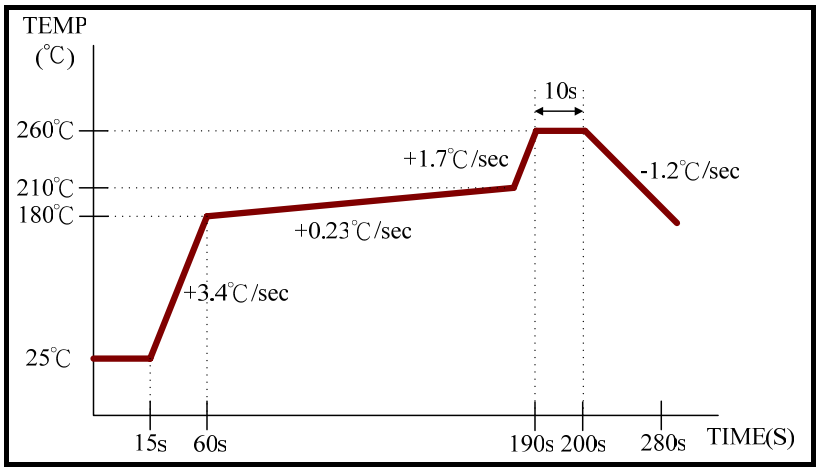
Lot Number is the last two numbers

For Example:

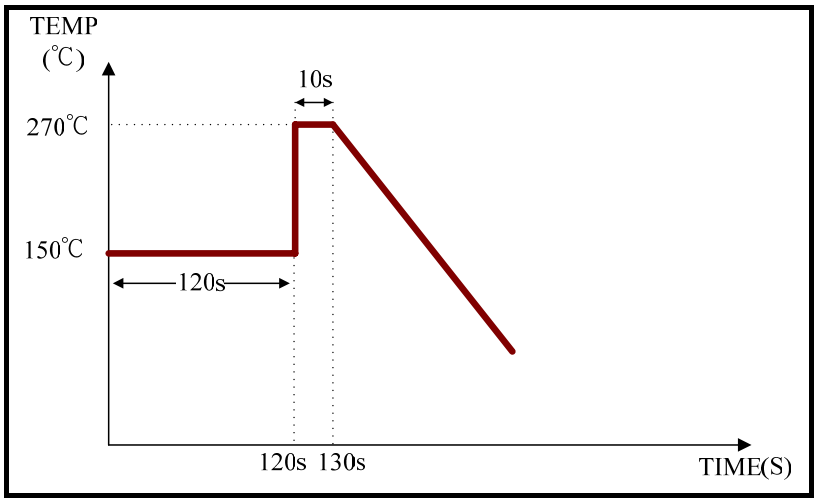
A3311C62
Lot Number

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (VCC) ---------- +30V
Current Shunt Regulator Common Mode Inputs Voltage ---------- -0.3V ~ 30V
Current Shunt Regulator differential Inputs Voltage (VIP – VIN) ---------- -30V ~ 1.5V
CSO Voltage ---------- -0.3V ~ V_{CC}
FPO Sink Current ---------- +40mA
FPO Off Voltage ---------- +30V
Cathode Voltage ---------- +30V
Cathode Continuous Current---------- -100mA~+150mA
Reference Input Current ---------- -50uA~+1mA
Operating Junction Temperature (T_J)---------- +150℃
Operating Junction Range (T_A)---------- -20℃~ +105℃
Storage Temperature Range (Ts) ---------- -55℃~ +150℃
Power Dissipation (SOP8, T_A=25℃) ---------- 570mW
(P-DIP8,T_A=25℃)---------- 900mW
SOP8 Lead Temperature (IR Re-flow soldering，10 sec) ---------- +260℃
PDIP8 Lead Temperature (Wave soldering，10 sec) ---------- +270℃



IR Re-flow Temperature vs. Second Curve



Wave Soldering Temperature vs. Second Cure

DC ELECTRICAL CHARACTERISTICS

(T_A= -20℃~+105℃, VCC=V_{IP}=12V, RG1=RG2=5K,R_L=125KΩ, unless otherwise noted)

Current Shunt Comparator section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Full Scale Sense Voltage	V_{SENSE}	$V_{SENSE}=V_{IP}-V_{IN}$		100	500	mV
Common-Mode Input Voltage	V_{CM}		2.7		30	V
Common-Mode Rejection	CMRR	V_{IP}=2.7V to 30V, V_{SENSE}=50mV	100	120		dB
Input Offset Voltage vs temp	$V_{OFFSET(ta)}$	-20℃ to +105℃		4	10	μV/℃
Input Offset Voltage vs V_{CC}	$V_{OFFSET(vcc)}$	V_{IN}=2.7V to 30V, V_{SENSE}=50mV		2.5	10	μV/V
Input Bias Current	I_{BIAS}	$V_{IP}=V_{IN}$=12V		2		μA
Non-linearity Error	NLE	V_{SENSE}=10mV to 150mV			±2	%
Total Output Error	TOE	V_{SENSE}=100mV			±2	%
Output Impedance	R_L	-		1||5		GΩ||pF
Voltage Swing to V_{CC}	V_{SCC}	-		V_{CC}-0.8		V
Voltage Swing to V_{CM}	V_{SCM}	-		V_{CM}-0.8		V
Bandwidth	BW	RG1=RG2=5K R_L=125KΩ		32		kHz
Settling Time	t_S	RG1=RG2=5K 5V Step, R_L=125KΩ		30		μS
Total Output-Current Noise	I_{NOISE}	BW=100KHz		3		nA
Operating Voltage Range	V_{CC}	-	2.7		30	V
Operating Temperature Range	T_A	-	-20		+105	℃

Shutdown Comparator section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Common-Mode Voltage (CSO)	V_{CM}	-	-0.3	-	V_{CC}-1.5	V
Voltage Gain	A_V	-	50	200	-	V/mV
Large Signal Response Time	T_R	-	-	300	-	nS
Response Time	Tr	-	-	1.3	-	μS
FPO Sink Current	I_{SINK}	Vcso>1.3V V_{FPO}≧ 1.0V	20	-	-	mA
FPO Saturation Voltage	V_{SAT}	Vcso>1.3V I_{SINK} ≦ 10mA	-	-	1	V
FPO Leakage Current	$I_{L(FPO)}$	Vcso<1.0V V_{FPO}= 30V	-	0.1	1	μA
CSO Threshold Voltage (V_{FPO} Switch High to Low)	V_{TH}	T_A=25℃	1.238	1.25	1.263	V
		T_A=-20℃~+105℃	1.225		1.275	
Hysteresis Voltage	V_{HYS}	V_{FPO} Switch High to Low		100		mV

DC ELECTRICAL CHARACTERISTICS (Cont.)

Test conditions: Ta= -20℃~+105℃, VCC=12V, unless otherwise noted

Voltage Shunt Regulator section

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Reference Voltage	V_{REF}	$V_{KA}=V_{REF}, I_{KA}=10mA$		2.487	2.5	2.513	V
V Reference vs. Temperature	V_{REF}	$V_{KA}=V_{REF}$, $I_{KA}=10mA$ T_A=-20℃~+105℃				30	mV
Line Regulation	$\Delta V_{REF}/\Delta V_{KA}$	I_{KA}=10mA	V_{KA} =10V~ V_{REF}		-1.4	-2.0	mV/V
			V_{KA}=30V~ 10V		-1.0	-2.0	
Reference Current	I_{REF}	R1=10KΩ,R2=∞ I_{KA}=10mA			0.5	4.0	μA
I Reference vs. Temperature	ΔI_{REF}	R1=10KΩ,R2=∞ I_{KA}=10mA, Ta=Full range			0.4	1.2	μA
Minimum Cathode Current for Regulation	$I_{KA(MIN)}$	$V_{KA}=V_{REF}$			0.1	0.5	mA
Dynamic Impedance	$\|Z_{KA}\|$	$V_{KA}=V_{REF}$, ΔI_{KA}=1mA~100mA Frequency < 1KHz			0.2	0.5	Ω

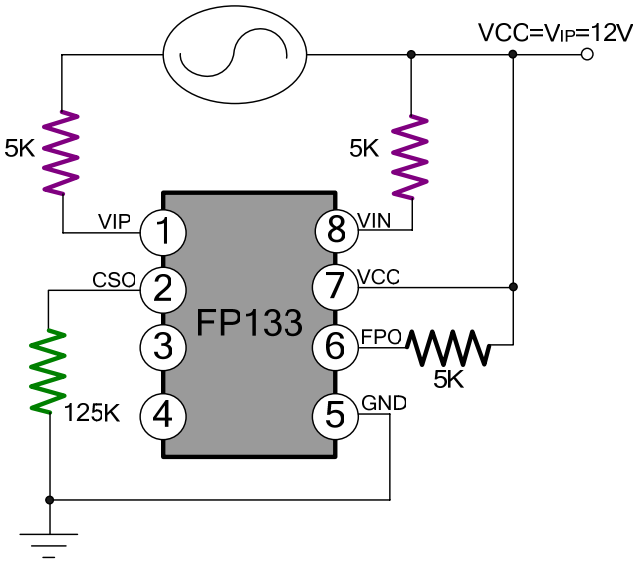
Total device section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Off IC Current	I_{CC}	V_{CC}=30V	-	0.4	-	mA

AC ELECTRICAL CHARACTERISTICS

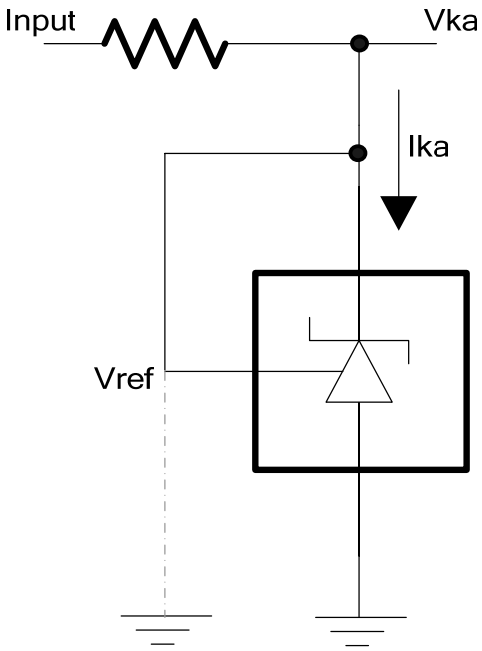
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
FPO Falling Delay Time	t_{fd}	See Test Circuit		6.4		μS
FPO Rising Delay Time	t_{rd}	See Test Circuit		4.4		μS

PARAMETER MEASUREMENT INFORMATION

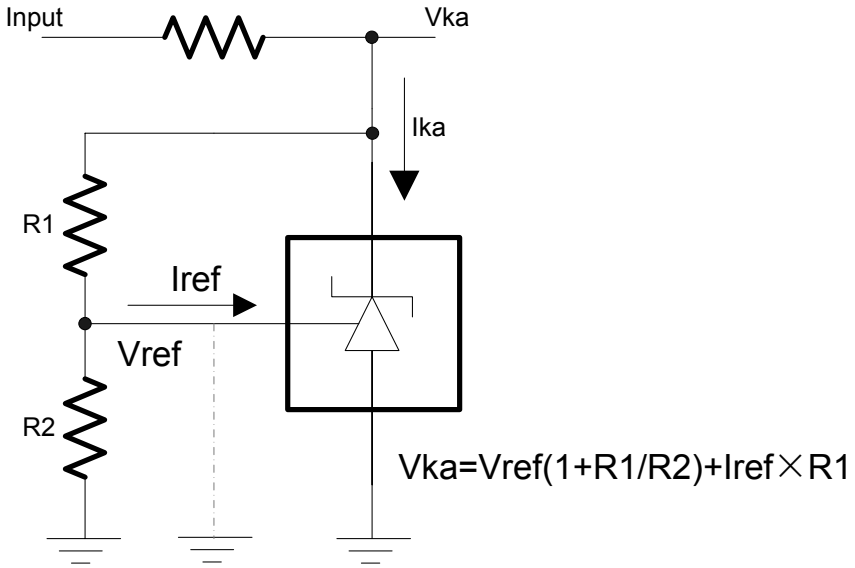


Test Circuit

PARAMETER MEASUREMENT INFORMATION(cont.)

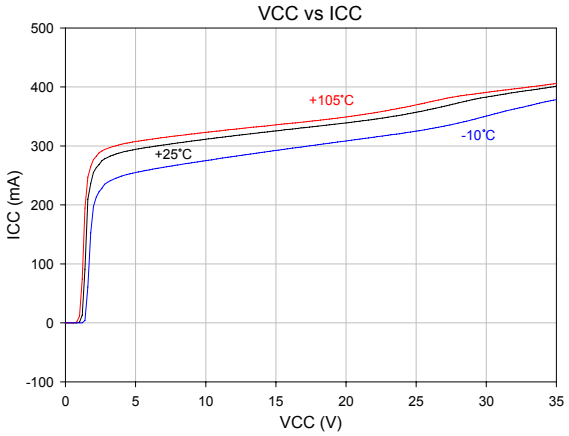


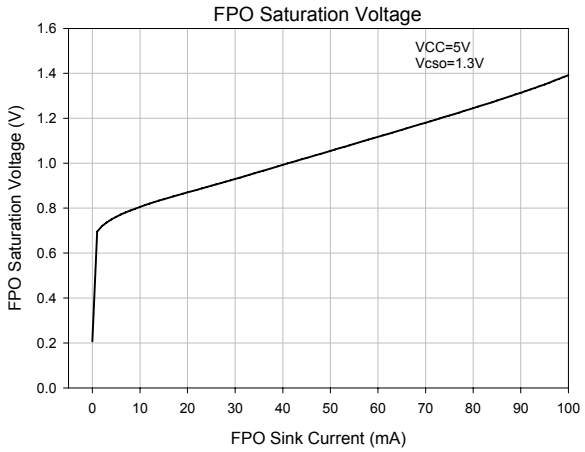
Test Circuit for Vka=Vref

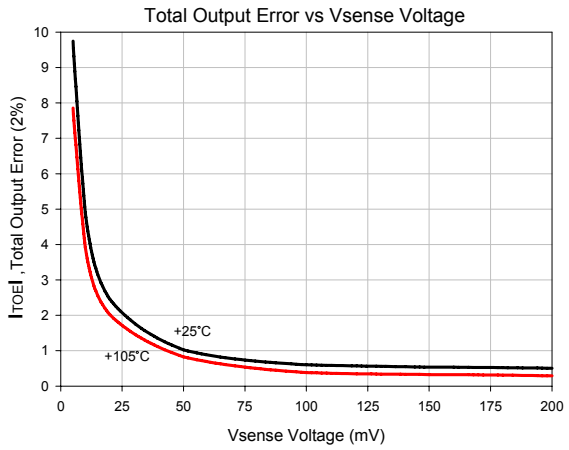


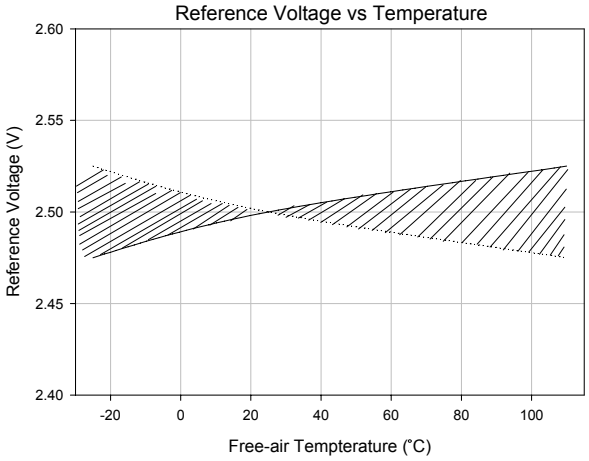
Test Circuit for Vka>Vref

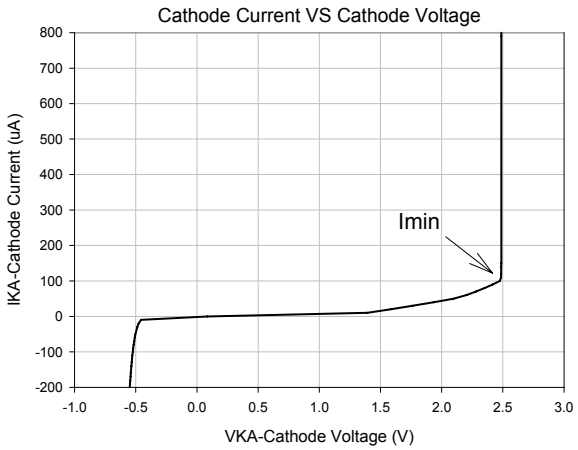
TYPICAL CHARACTERISTICS (Ta=+25℃,VCC=12V,VIP=12V, unless otherwise noted)

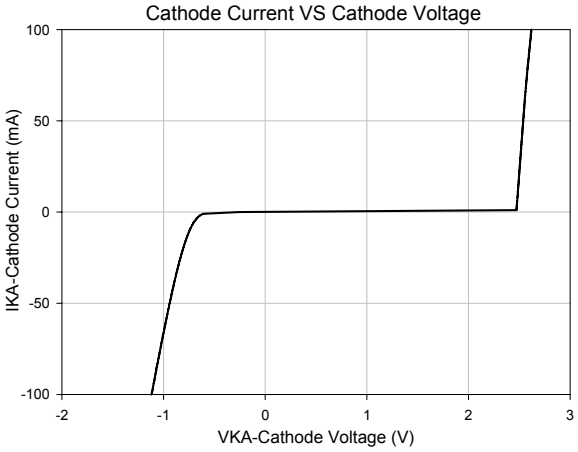






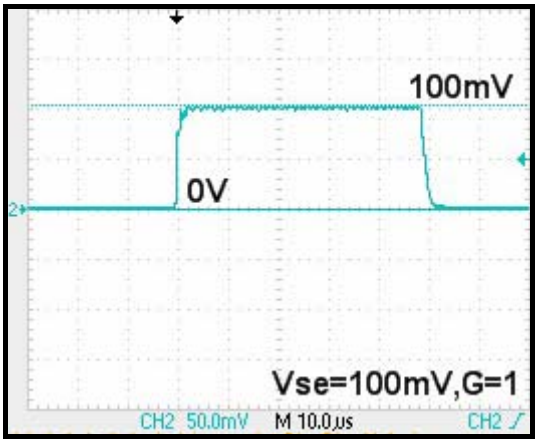


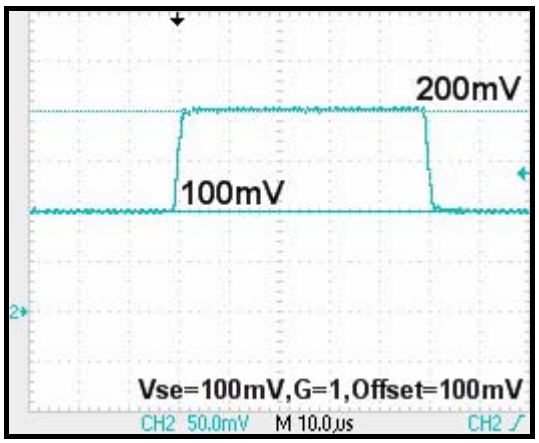


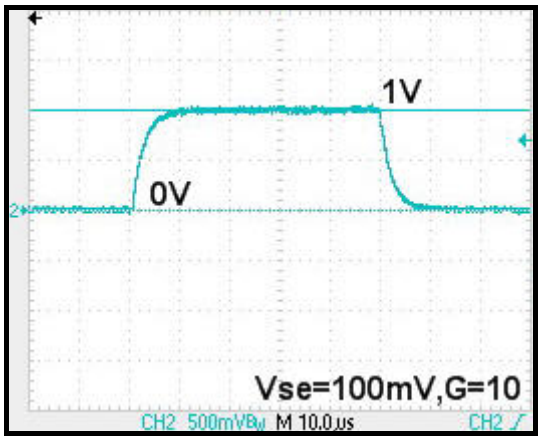


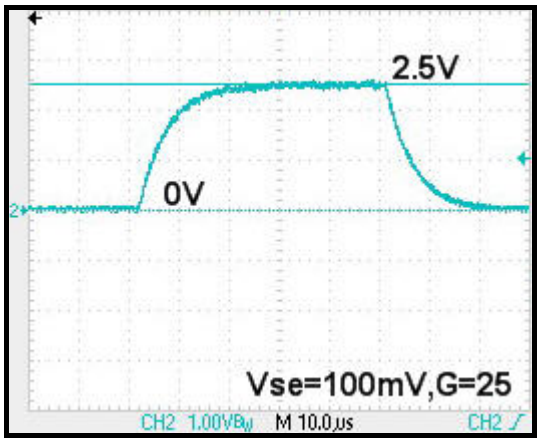
TYPICAL CHARACTERISTICS (Ta=+25℃,VCC=12V,VIP=12V, unless otherwise noted)

RG1=RG2=5K

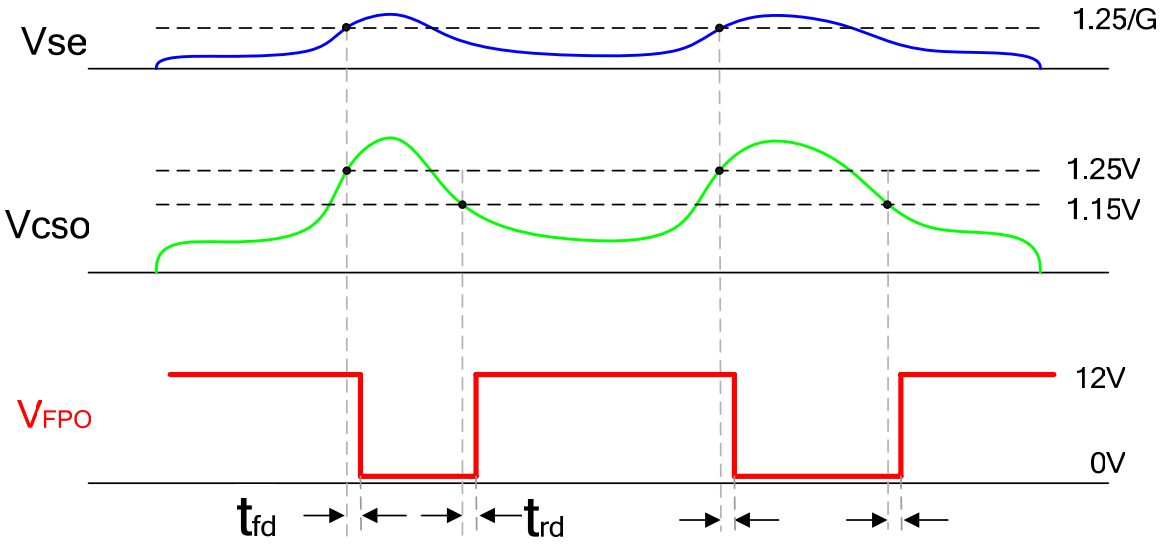








Time Waveform Chart



DETAILED DESCRIPTION

Current Shunt Regulator

The figure shows the **FP133** current shunt block, when the load current (I_S) flows from power supply and a dropout voltage (V_{IN}^+-V_{IN}^-) at the sense resistor (R_S).

Assume internal NPN transistor collector current is same as emitter current (I_O) and VIP is very close VIN, the **FP133** transfer function is:

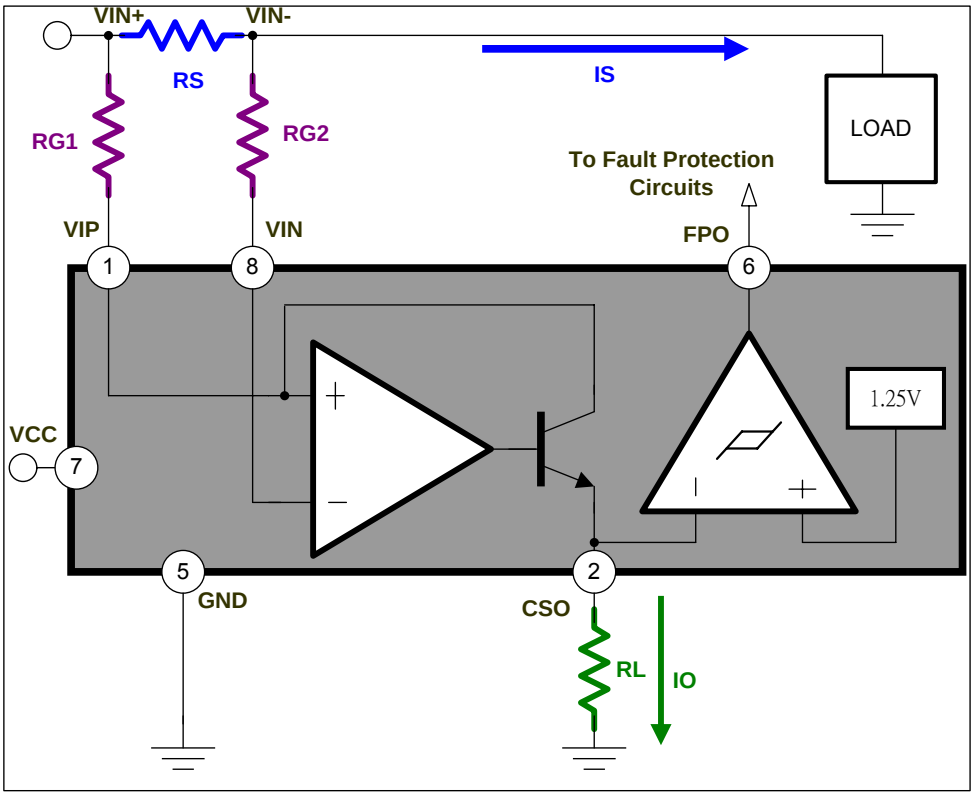
$$I_O = \frac{V_{IN}^{+} - V_{IN}^{-}}{RG1} \quad \text{----- (1)}$$

In the figure, the (V_{IN}^+-V_{IN}^-), is equal to $I_S \cdot R_S$ and the current shunt output voltage (CSO) is equal to $I_O \cdot R_L$. The final transfer function for rail current measurement in this application is:

$$V_{CSO} = G * I_S * R_S \quad \text{---- (2)}$$

$$G = R_L / RG1 \quad \text{---- (3)}$$

In **FP133** internal circuits, the CSO output is connected with inverting input of shutdown comparator, when the voltage of CSO is higher than the internal reference voltage (**1.25V**), the FPO pin is switching from high to low state, this signal can be used for OLP protection control.



NOTE

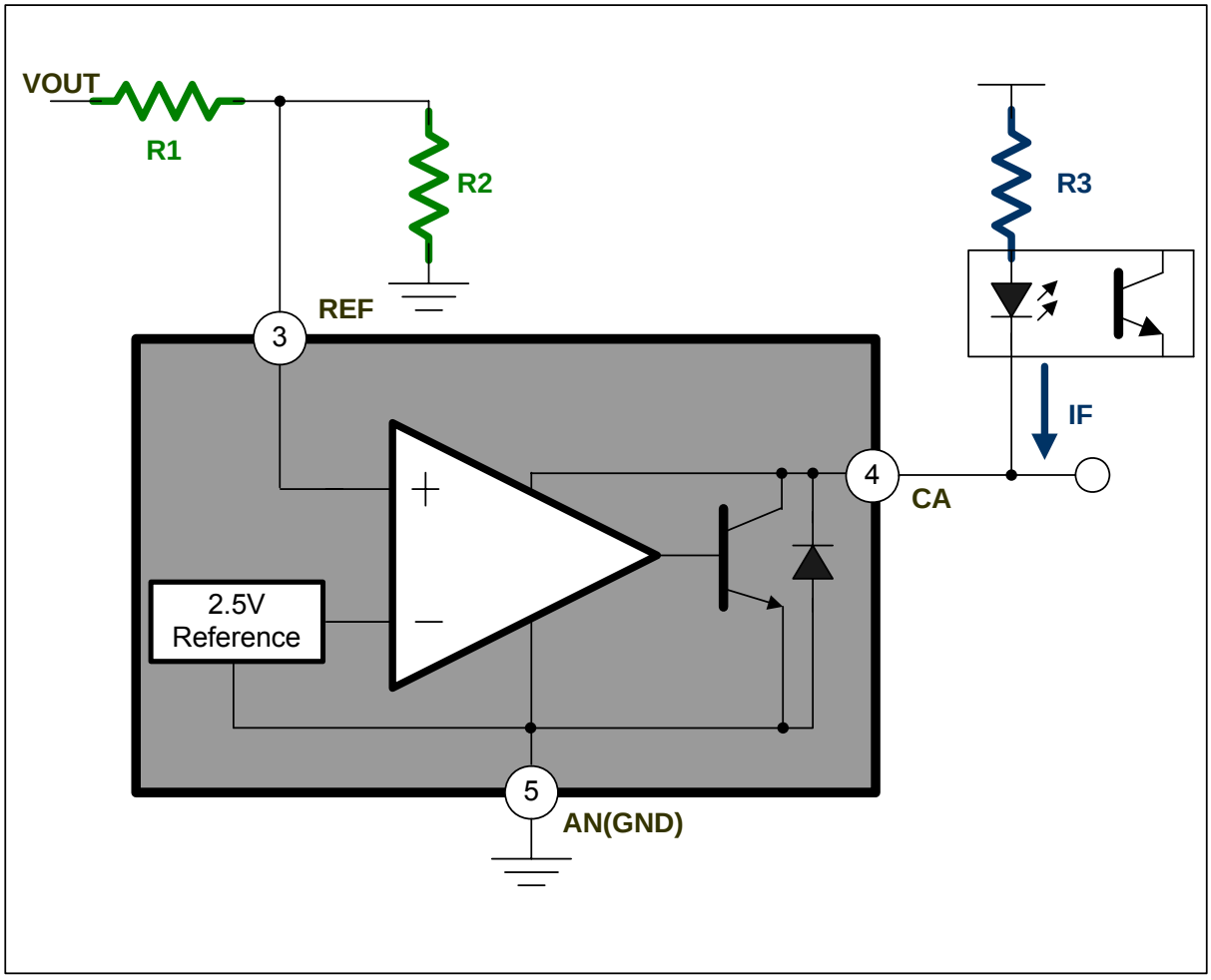
1. The minimum operating voltages of VCC, VIP and VIN are 2.7V, if these supply voltages are low than 2.7V, the transfer function at current shunt output (CSO) of **FP133** isn't correct.
2. Don't force a VIN voltage that is over 15V than VIP, this condition would generate a leakage current and an incorrect voltage at **FP133** output.

Voltage Shunt Regulator

The figure shows the **FP133** voltage shunt regulator, it has an internal reference **2.5V** connecting to the IN- of comparator and high cathode current sink ability for photo-coupler driving.

The VOUT formula is shown below:

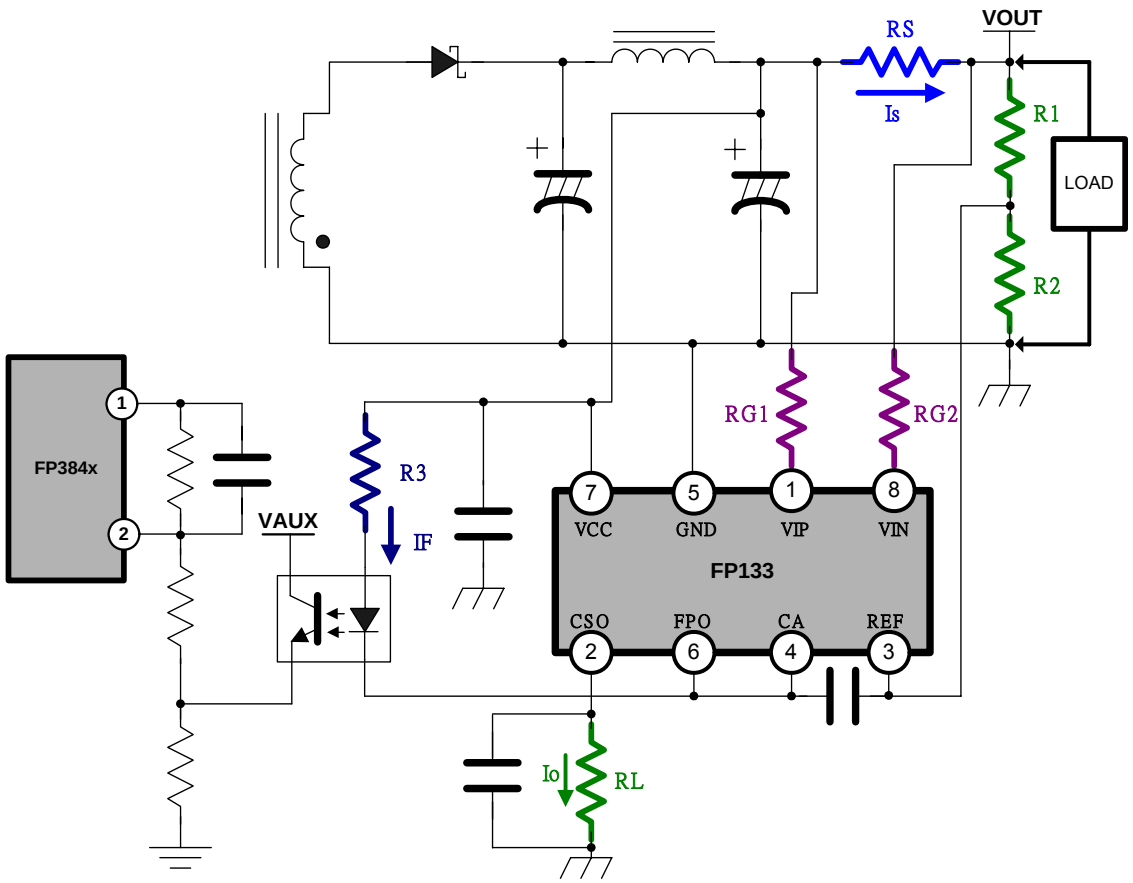
$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 2.5V \quad \text{---- (4)}$$



NOTE

1. To connecting a compensation network between CA and REF pins avoids output voltage has a high ring during light loading or transient.
2. AN pin must tie to IC GND pin for the same ground level.
3. R3 is selectable for dynamic loading feedback.

APPLICATION NOTE



Adaptor secondary Voltage Feedback / Over Loading Protection circuit

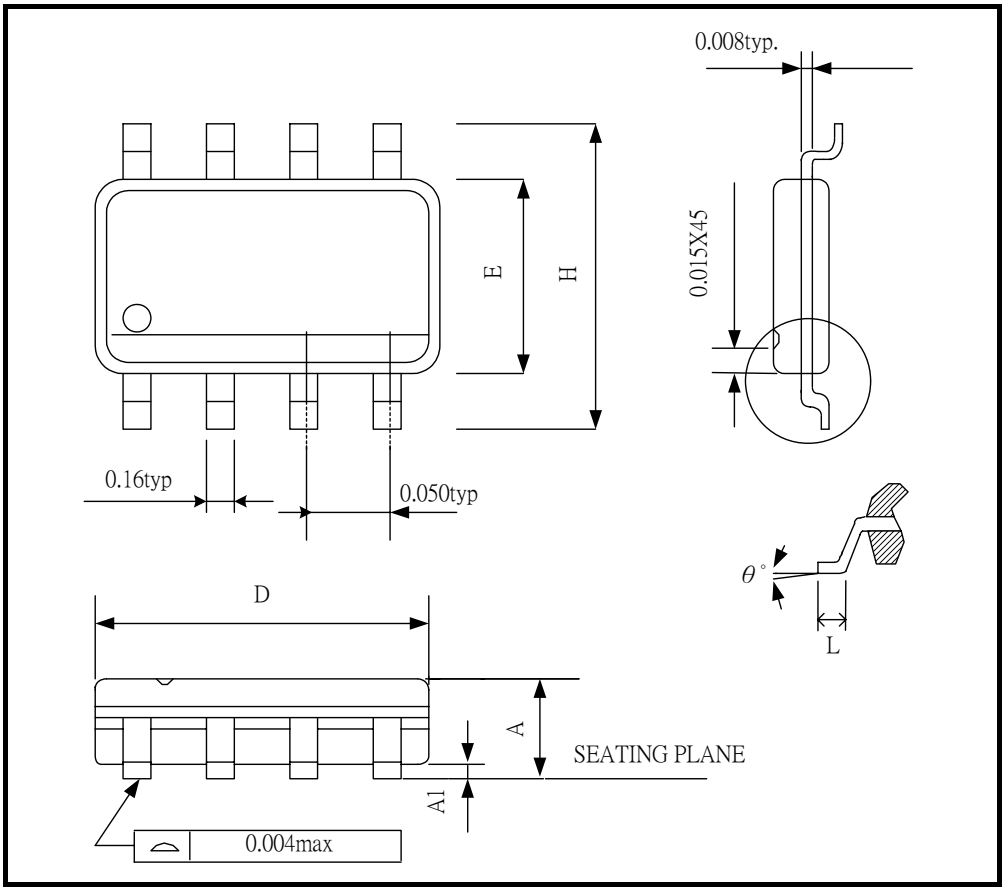
The above circuits are a simple application for AC/DC adaptor over loading protection (OLP) function with output voltage feedback.

For example, when load current (I_S) increases, the **FP133** CSO voltage would increase as formula (2) until the internal shutdown comparator IN- connecting to CSO pin is higher than **1.25V** reference, that has a sink current (I_{OUT}) flowing through the photo-coupler, and **FP384x** PWM IC will change the NMOS drive terminal to a minimum duty cycle current limitation for secondary over current protection, and primary side auxiliary voltage can not maintain the **FP384x** power supply, the **FP384x** will be shutdown until AC line start-up voltage is re-start the PWM IC.

The **FP133** has a voltage shunt regulator would response the output voltage change with R1 and R2, the feedback current will flow from photo-coupler to **FP133** CA pin (pin4), and generate the feedback signal voltage to PWM IC **FP384x**.

PACKAGE OUTLINE

SOP8



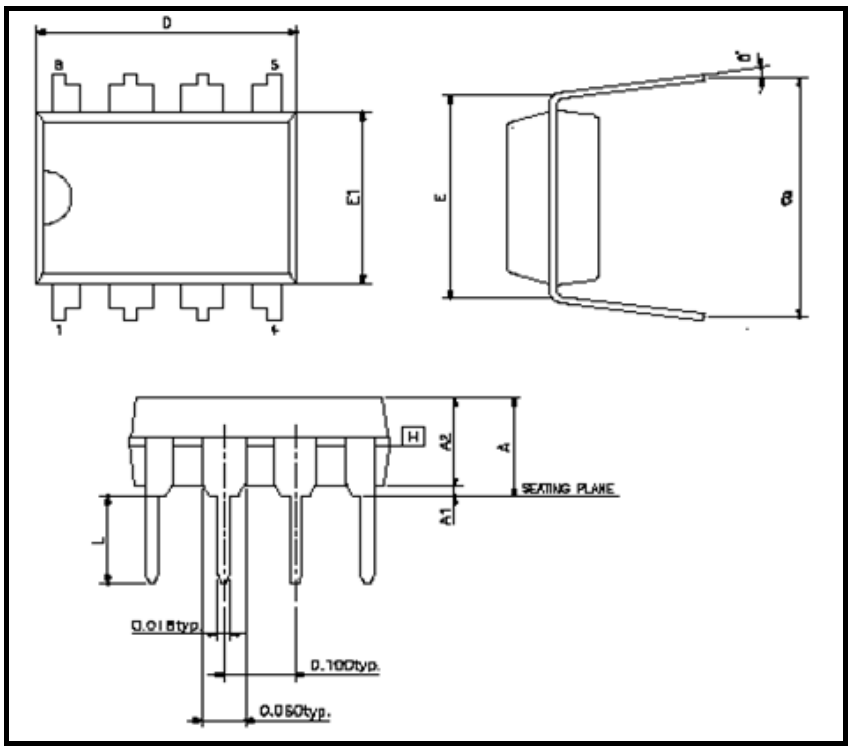
SYMBOLS	MIN	MAX
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT:INCH

NOTE:

1. JEDEC OUTLINE:MS-012 AA。
2. DIMENSIONS “D” DOES NOT INCLUDE MOLD FLASH,PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.0.06in) PER SIDE。
3. DIMENSIONS “E” DOES NOT INCLUDE INTER-LEAD FLASH,OR PROTRUSIONS INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.0.10in) PER SIDE。

PDIP8



SYMBOLS	MIN.	NOR.	MAX.
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ	0	7	15

UNIT:INCH

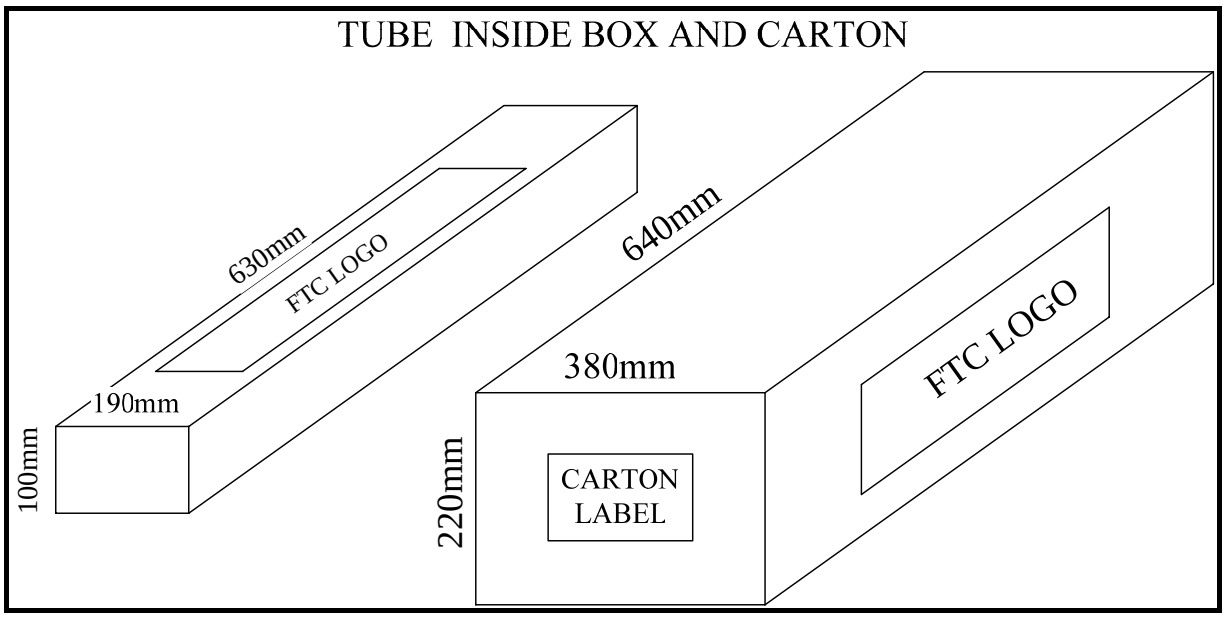
Note:

1. JEDEC OUTLINE:MS-001 BA。
2. “D”、”E1” DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH。
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED。
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTIDN。
5. DISTANCE BETWEEN LEADSINCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM。
6. DATUM PLANE H CONINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY。

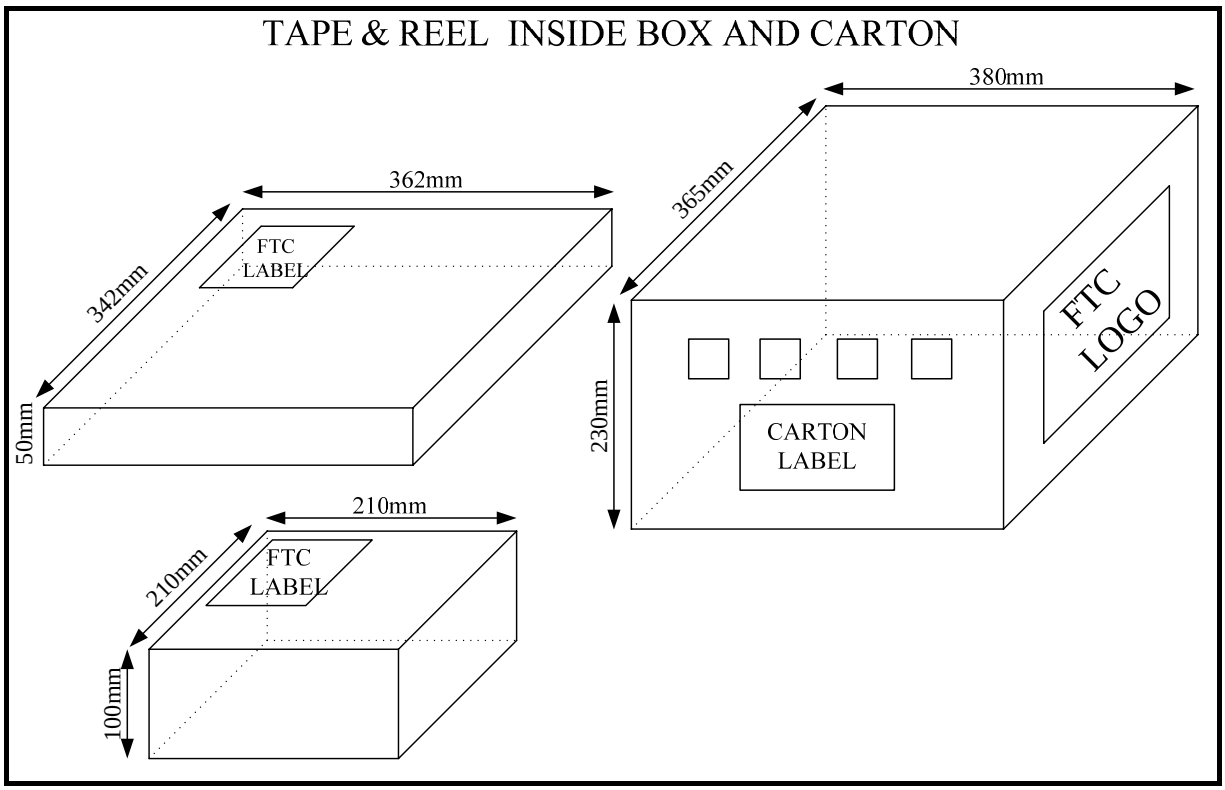
PACKING SPECIFICATIONS

BOX & CARTON DIMENSION

PDIP8 & SOP8



SOP8 & SOT-25



PACKING QUANTITY SPECIFICATIONS

SOP8	PDIP8
2500 EA / REEL	60 EA/TUBE
1 REELS / INSIDE BOX	60 TUBES / INSIDE BOX
4 INSIDE BOXES / CARTON	4 INSIDE BOXES / CARTON

LABEL SPECIFICATIONS

TAPPING & REEL

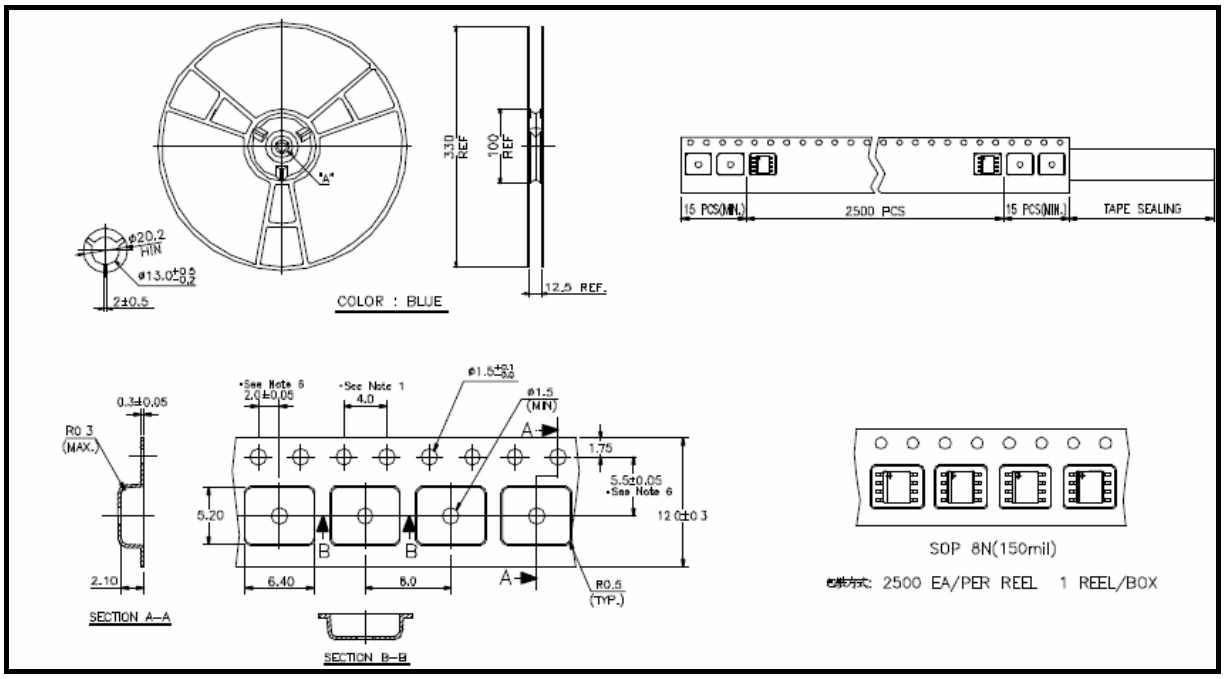
Feeling Technology Corp
Product:FP133DR-LF
Lot NO: A3311CXX-L
D/C: 6Xx-XXL
Q`ty: 2500
無鉛
Lead Free

CARTON

Feeling Technology Corp
Product Type: FP133DR-LF
Lot No: A3311CXX-L
Date Code: 6Xx-XXL
Package Type:SOP8
Marking Type:Laser
Total Q`ty: 10,000
無鉛
Lead Free

CARRIER TAPE AND REEL DIMENSIONS

SOP8



Note:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE 0.2mm。
2. COMBER NOT TO EXCEED 1mm IN 100mm。
3. MATERIAL:ANTI-STATIC BLOCK ADVANTEK POLYSTYRENE。
4. A_0 AND B_0 MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET。
5. K_0 MEASURED FROM A PLANE AN THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER。
6. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET，NOT POCK