SELF-OSCILLATING HALF-BRIDGE DRIVER

1. Description

iT2153S is a half-bridge driver with programmable oscillator within a SOP-8L package to drive both, lower MOSFET and floating upper MOSFET. It is suitable for electronic ballast of fluorescent lamp, either hot or cold cathode. It is equipped with internal clamp of about 15 V zener diode, so using a limited supply power; the V_{CC} voltage is easily regulated. The relaxation oscillator frequency is easily adjusted using a capacitor and a resistor on C_T and R_T pins respectively. For proper operation assurance and low power start-up, it is designed with internal under voltage lockout (UVLO), so it takes little current for supply capacitor voltage to builds up. Once it reaches UVLO on, it starts operate, and it will turn off only if the voltage is below UVLO off, so between these voltages the proper operation is guaranteed. Therefore it only needs very few external components.

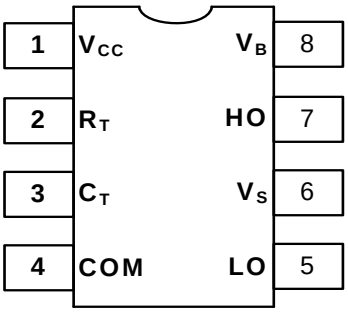
2. Features

- Integrated 600 V half-bridge gate driver
- 15.6 V zener clamp on V_{CC}
- True micro-power start up
- Low temperature coefficient dead-time
- Shutdown feature (1 / 6 V_{CC}) on C_T pin
- Increased under-voltage lockout Hysteresis
- Lower power level-shifting circuit
- Constant LO, HO pulse widths at startup
- Lower di / dt gate driver for better noise immunity
- Low side output in phase with R_T
- Excellent latch immunity on all inputs and outputs

3. Applications

- CFL ballast
- CCFL ballast
- T5 ballast

4. Pin Assignments



8 Lead SOIC

5. Marking Information

Product Name	Marking
iT2153S	iT2153S XXXXX X : Date Code

6. Ordering Code

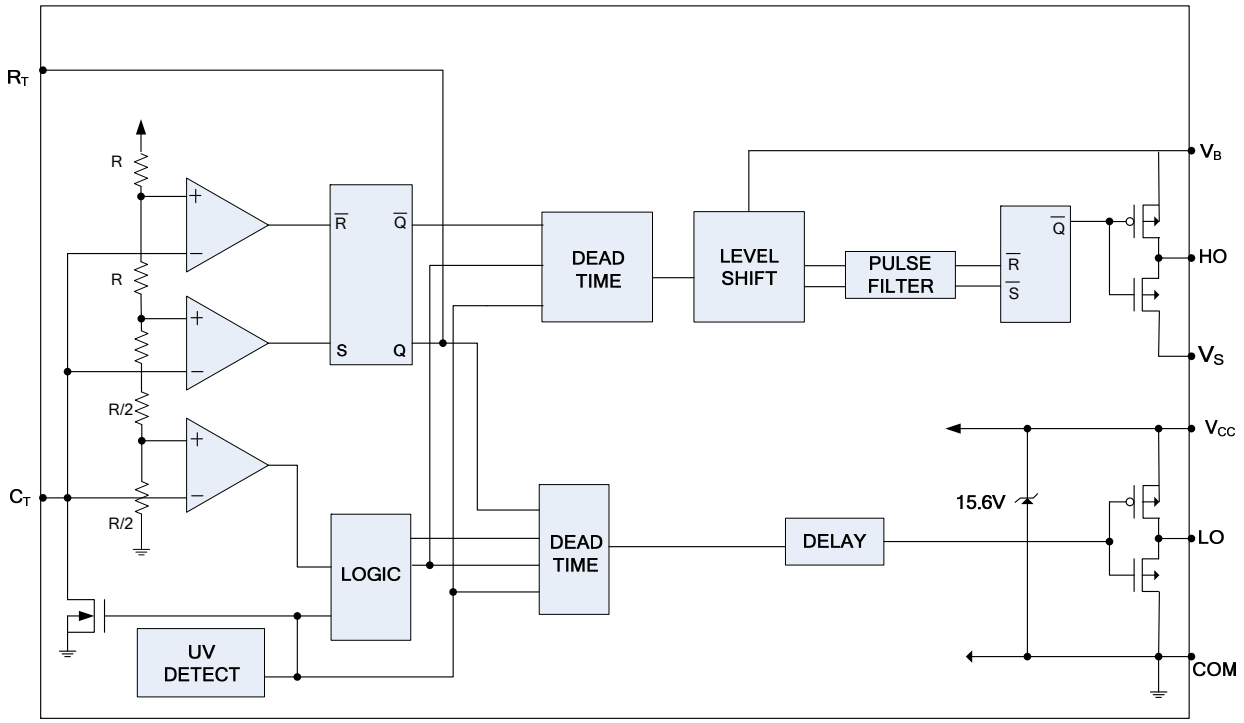
iT2153S□ └── Assembly Material	Assembly Material G: Halogen and Lead Free Device

Note: inergy defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

7. Pin Definitions

Pin No.	Symbol	Description
1	V_{CC}	Logic and internal gate drive supply voltage
2	R_T	Oscillator timing resistor input
3	C_T	Oscillator timing capacitor input
4	COM	IC power and signal ground
5	LO	Low side gate driver output
6	V_S	High voltage floating supply return
7	HO	High side gate driver output
8	V_B	High side gate driver floating supply

8. Block Diagram



9. Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits and beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	625	V
V_S	High side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage	- 0.3	V_{CC} + 0.3	
V_{RT}	R_T pin voltage	- 0.3	V_{CC} + 0.3	
V_{CT}	C_T pin voltage	- 0.3	V_{CC} + 0.3	
I_{CC}	Supply current (note)	—	20	mA
I_{RT}	R_T pin current	- 5	5	
dV / dt	Allowable offset voltage slew rate	- 50	50	V / ns
P_D	Maximum power dissipation (8 lead SOIC) @ $T_A \leqq$ + 25 ℃	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient (8 lead SOIC)	—	200	℃ / W
T_J	Junction temperature	- 55	150	℃
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Note： This supply pin should not be driven by a DC, which is low impedance power source greater than the V_{CLAMP}.

10. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	- 3.0	600	
V_{CC}	Supply voltage	V_{CCUV+} + 0.1 V	V_{CLAMP}	
I_{CC}	Supply current	—	5	mA
T_J	Junction temperature	- 40	125	℃

11. Static Electrical Characteristics

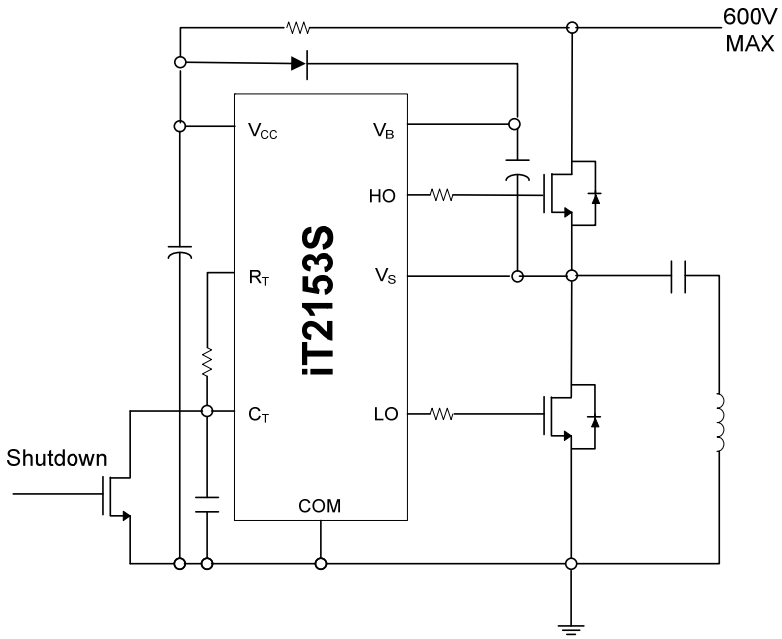
V_{BIAS} (V_{CC}, V_{BS}) = 12 V, C_T = 1 nF, V_S = 0 V and T_A = 25 ℃ unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to COM and are applicable to the respective output leads : HO or LO. C_{LO} = C_{HO} = 1 nF.

Symbol	Definition	Min	Typ	Max	Unit	Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} under-voltage lockout threshold	-	11.4	-	V	
V_{CCUV-}	Falling V_{CC} under-voltage lockout threshold	-	9.8	-		
$V_{CCUVHYS}$	V_{CC} under-voltage lockout Hysteresis	-	1.6	-		
I_{QCCUV}	Micro-power startup V_{CC} supply current	-	103	-	μA	$V_{CC} \leqq V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	-	400	-		$V_{CC} \geqq V_{CCUV+}$
V_{CLAMP}	V_{CC} zener clamp voltage	-	15.6	-	V	I_{CC} = 5 mA
Floating Supply Characteristics						
I_{QBS}	Quiescent V_{BS} supply current	-	20	-	μA	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold	-	6.5	-	V	
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold	-	5.5	-		
I_{LK}	Offset supply leakage current	-	-	50	μA	V_B = V_S = 600 V
Oscillator I / O Characteristics						
f_{OSC}	Oscillator frequency	-	18.6	-	kHz	R_T = 36 K
		91	97	103		R_T = 6.2 K
d	R_T pin duty cycle	-	50	-	%	f_{OSC} < 103 kHz
I_{CT}	C_T pin current	-	0.02	1	μA	
I_{CTUV}	UV-mode C_T ramp voltage threshold	-	0.70	1.2	mA	V_{CC} = 7 V
V_{CT+}	Upper C_T ramp voltage threshold	-	8.2	-	V	
V_{CT-}	Lower C_T ramp voltage threshold	-	3.86	-		
V_{CTSD}	C_T voltage shutdown threshold	-	1.9	-		
V_{RT+}	High-level R_T output voltage, V_{CC} - V_{RT}	-	10	50	mV	I_{RT} = - 100 μA
		-	100	300		I_{RT} = - 1 mA
V_{RT-}	Low-level R_T output voltage	-	10	50		I_{RT} = 100 μA
		-	100	300		I_{RT} = 1 mA
V_{RTUV}	UV-mode R_T ramp voltage	-	0	100		$V_{CC} \leqq V_{CCUV-}$
V_{RTSD}	SD-mode R_T ramp voltage, V_{CC} - V_{RT}	-	10	50		I_{RT} = - 100 μA, V_{CT} = 0 V
		-	100	300		I_{RT} = - 1 mA, V_{CT} = 0 V

11. Static Electrical Characteristics (cont.)

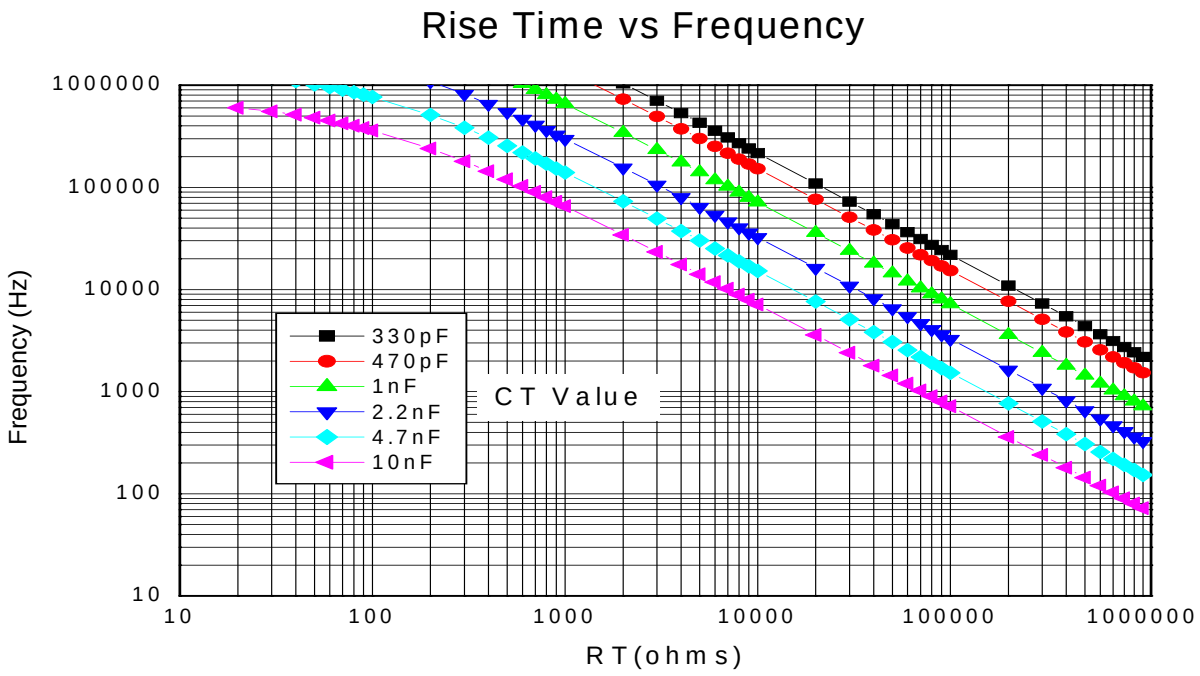
Symbol	Definition	Min	Typ	Max	Units	Conditions
Gate Driver Output Characteristics						
V_{OH}	High-level output voltage, V_{BIAS} - V_O	-	0	100	mV	I_O = 0 A
V_{OL}	Low-level output voltage, V_O	-	0	100		
V_{OLUV}	UV-mode output voltage, V_O	-	0	100		I_O = 0 A , $V_{CC} \leqq V_{CCUV-}$
t_r	Output rise time	-	80	-	ns	V_{CC} = 15 V C_{LO} = C_{HO} = 1 nF
t_f	Output fall time	-	56	-		
t_{sd}	Shutdown propagation delay	-	650	-		
t_d	Output dead-time	-	1.26	-	μs	
I_{O+}	Output source current	-	220	-	mA	
I_{O-}	Output sink current	-	300	-		

12. Application Circuit



13. Recommended Component Values

Symbol	Conditions	Min	Max	Unit
R_T	Timing resistor value	10	—	kΩ
C_T	C_T pin capacitor value	330	—	pF



14. Timing Diagram

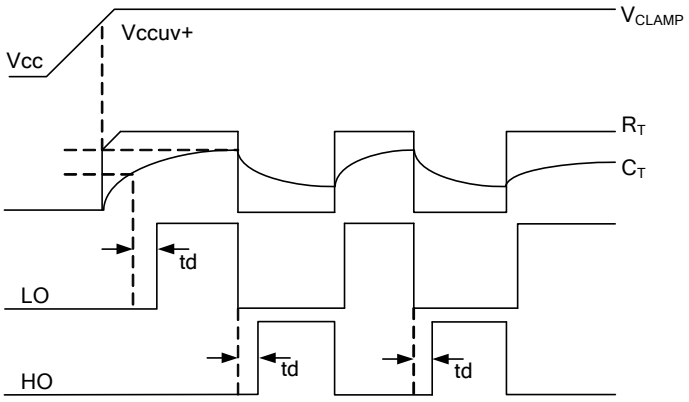


Figure 1. Input / Output Timing Diagram

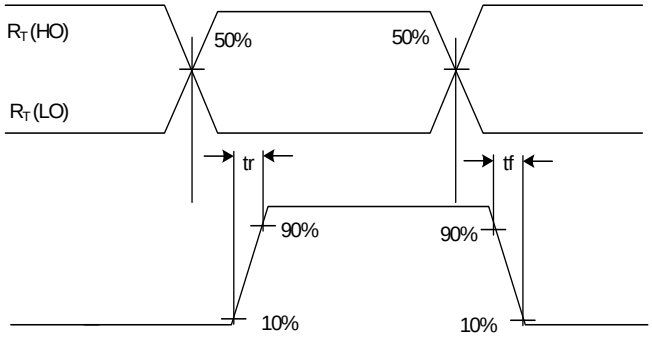


Figure 2. Switching Time Waveformse

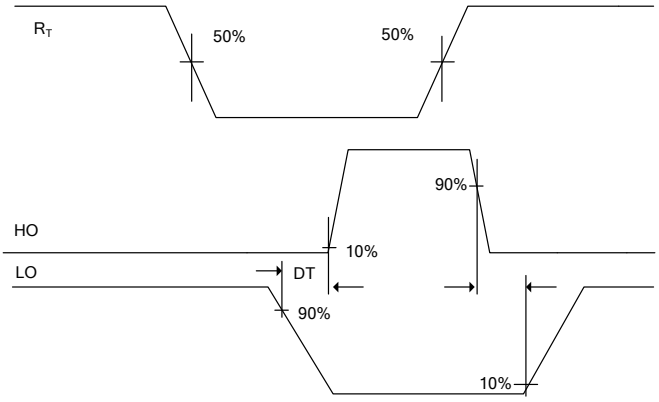


Figure 3. Dead-Time Waveform Definitions

15. Typical Characteristics

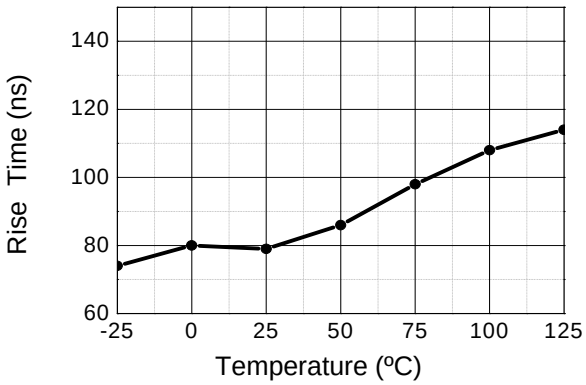


Figure 1. Rise Time vs Temperature

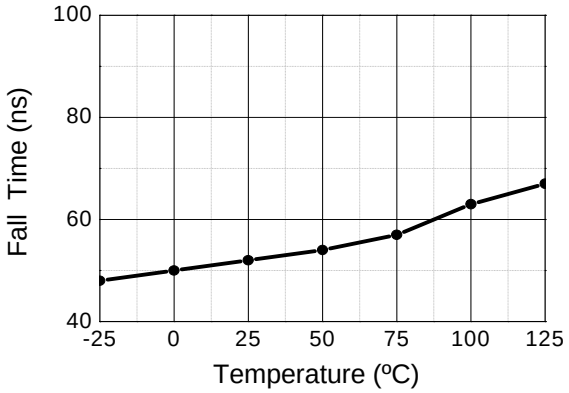


Figure 2. Fall Time vs Temperature

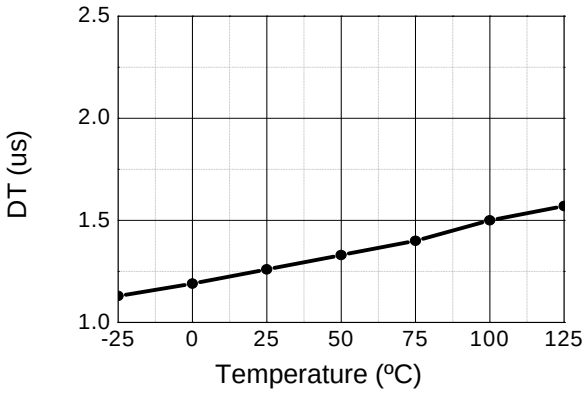


Figure 3. Dead Time vs Temperature

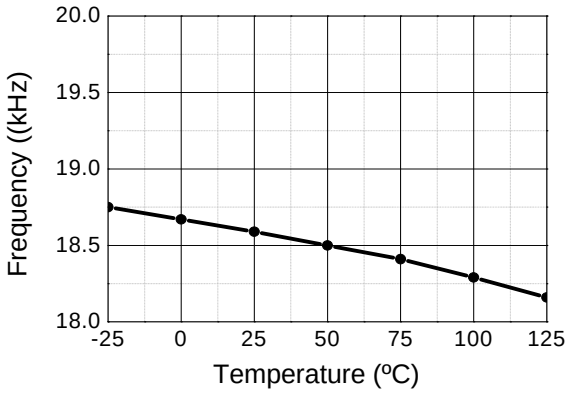


Figure 4. Frequency vs Temperature

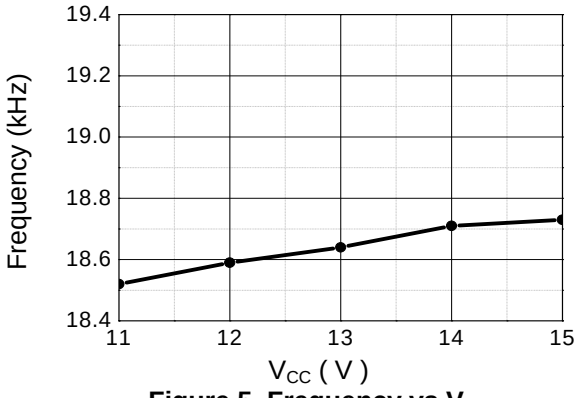


Figure 5. Frequency vs V_{CC}

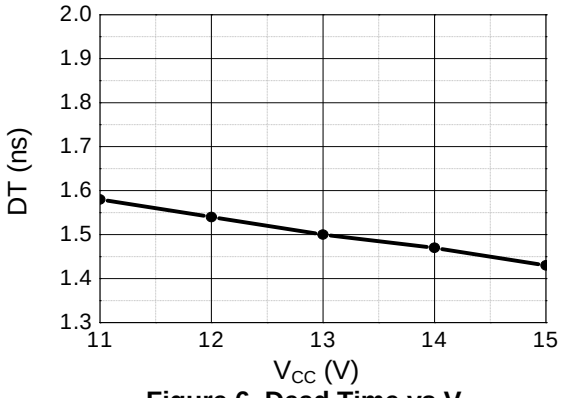
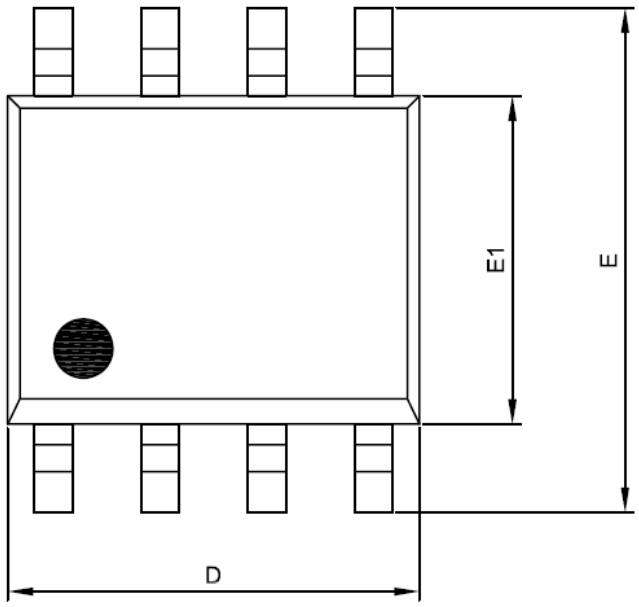
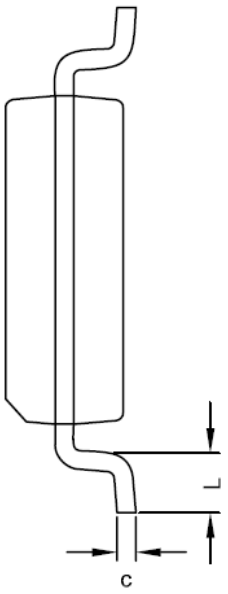


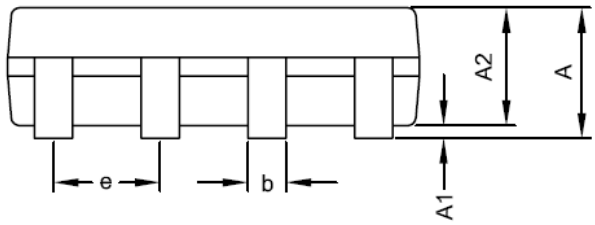
Figure 6. Dead Time vs V_{CC}

16. Package Dimensions

SOP- 8L







Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.