

1.5MHz, High-Efficiency 1.2A Synchronous Step-Down Converter in MSOP-10

Description

The FP6365 is a high efficiency, low-noise, DC-DC step-down pulse width modulated (PWM) converter. It is ideally suited for systems powered from a 1-cell Li-ion battery or from a 2- to 3-cell NiCd, NiMH, or alkaline battery. 100% duty cycle provides low dropout operation, extending battery life in portable systems. Switching frequency is internally set at 1.5MHz, allowing the use of small external surface mount inductors and capacitors. The internal synchronous switch increases efficiency and eliminates the need for an external schottky diode.

The device operates in one of four modes. Forced PWM mode operates at a fixed frequency regardless of the load. Synchronizable mode allows an external switch frequency to control and minimize harmonics. The FP6365 can be externally synchronized from 1MHz to 2MHz. To achieve highest efficiency over a wide load current range, the converter enters power saving (PFM) mode at light load. Shutdown mode places the device in standby, reducing quiescent supply current to less than 1 μ A.

The FP6365 is available in a space saving 10-pin MSOP package.

Pin Assignments

MS Package (MSOP-10)

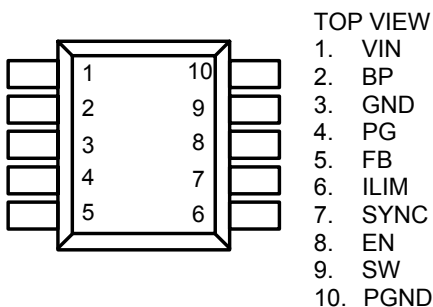


Figure 1. Pin Assignment of FP6365

Features

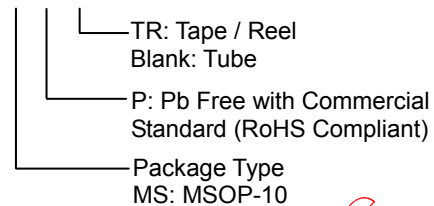
- Synchronous Rectification: Approach 95% Efficiency
- 2.5V to 5.5V Input Voltage Range
- The PFM Mode Operation for Improving Efficiency at Light Load
- Real Shutdown Isolated Load from Battery
- Very Low Quiescent Current at 30 μ A in PFM mode
- Internal Compensation Without External Capacitors and Resistors
- No Schottky Diode Required
- Low Dropout Operation: 100% Duty Cycle
- PWM/PFM Enable Control
- Fixed Frequency Operation at 1.5MHz
- Very Low Shutdown Current at 1 μ A (Max.)
- Small 10-Pin MSOP Package
- RoHS Compliant

Applications

- Cellular Phones
- Handheld Instruments
- Cordless Phones
- Wireless Handsets
- MP3 Portable Audio Players
- Battery Operated Devices

Ordering Information

FP6365



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Typical Application Circuit

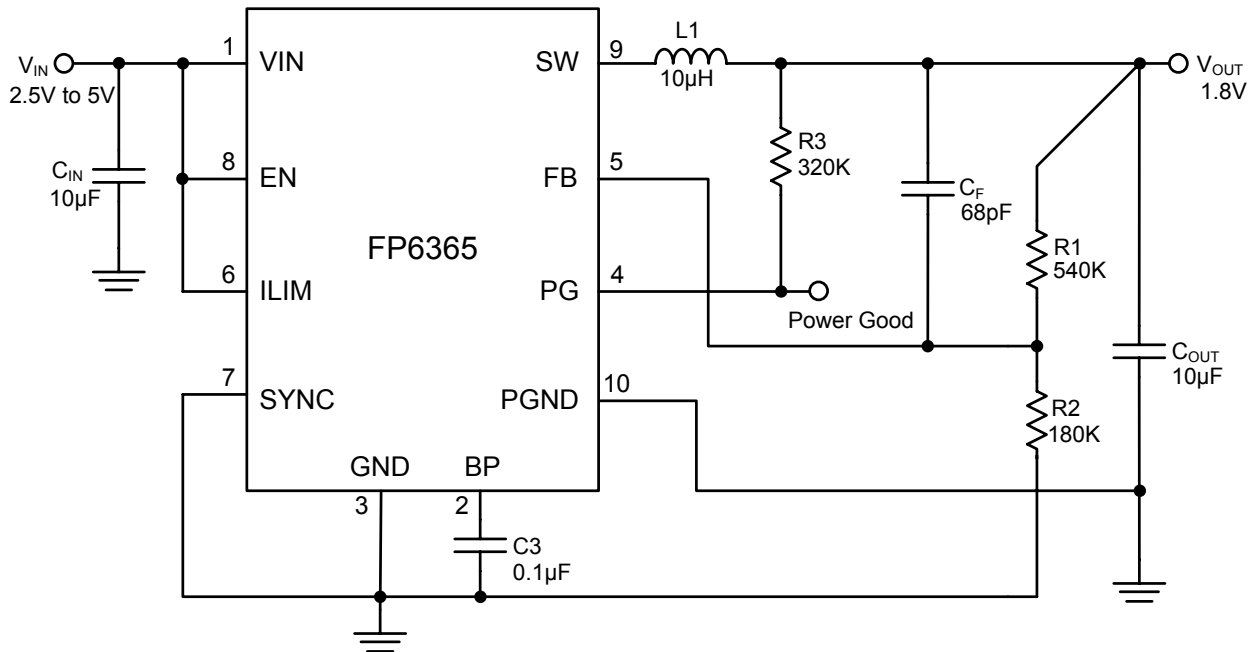


Figure 2. Typical Application Circuit of FP6365

Functional Pin Description

Pin Name	Pin Function
VIN	Supply voltage input. Input range from 2.5V to 5.5V. Bypass with a 10µF Capacitor
BP	Supply bypass pin. Internally connected to VIN. Bypass with a 0.1µF capacitor. Do not connect to an external power source other than VIN
GND	Ground
PG	Power good comparator output. The output goes active high when the output voltage is greater than 92% of the nominal value
FB	Feedback input.
ILIM	Current limit select input. Connect to GND for 0.9A current limit or to VIN for 1.6A current limit
SYNC	Input for synchronization to external clock signal. Synchronize the converter switching frequency to an external clock signal with CMOS level : SYNC=HIGH : Low-noise mode enabled, fixed frequency PWM operation is forced SYNC=LOW (GND) : Power saving mode enabled, PWM/PFM auto-switch operation is forced
EN	Enable pin. A logic high enables the converter, logic low forces the device into shutdown mode reducing the supply current to less than 1µA
SW	Inductor connection to the drains of the internal power MOSFETs.
PGND	Power ground.

Block Diagram

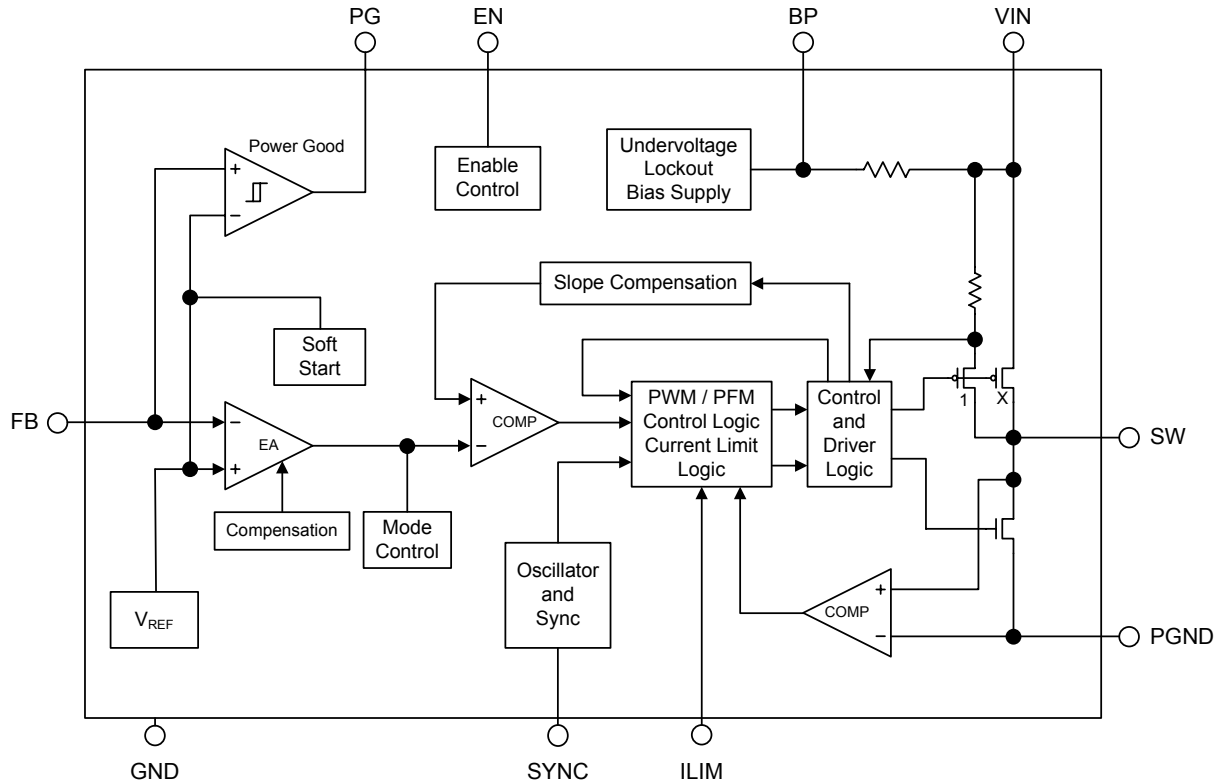


Figure 3. Block Diagram of FP6365

Absolute Maximum Ratings

- V_{IN}, BP, EN, SYNC, ILIM, PG to GND ----- -0.3V to + 6V
- BP to V_{IN} ----- -0.3V to + 0.3V
- PGND to GND ----- -0.3V to + 0.3V
- SW to PGND ----- -0.3V to + (V_{IN}+0.3V)
- FB to GND ----- -0.3V to + (V_{BP}+0.3V)
- Maximum Junction Temperature (T_J) ----- + 150°C
- Storage Temperature (T_{STG}) ----- -65°C to +150°C
- Power Dissipation @ T_A=25°C, MSOP-10 (P_D) ----- 630mW
- Package Thermal Resistance, MSOP-10 (θ_{JA}) ----- 160°C/W
- Lead Temperature (Soldering, 10sec.) ----- + 260°C

Note : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{IN}) ----- + 2.5V to + 5.5V
- Operation Temperature Range (T_{OPR}) ----- - 40°C to + 85°C

Electrical Characteristics

($V_{IN}=3.6V$, $EN=V_{IN}$, $T_A=25\text{ }^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Operating Input Voltage	V_{IN}		2.5		5.5	V
Output Voltage Range	V_O		0.8		V_{IN}	V
Operating Quiescent Current	I_Q	$I_O=0\text{mA}$, SYNC=GND (PFM mode enabled)		30	45	μA
Shutdown Current	I_{SD}	EN=GND		0.1	1	μA
EN High Level Input Voltage	V_{IH}		1.5			V
EN Low Level Input Voltage	V_{IL}				0.4	V
EN Input Leakage Current	I_{LKG}	EN=GND or V_{IN}		0.01		μA
Under Voltage Lockout Threshold	V_{UVLO}		1.2	1.65	1.95	V
P-Channel MOSFET On-Resistance	$R_{DS(ON)}$	$V_I = V_{GS} = 3.6V$, $I = 200\text{mA}$		330	480	m Ω
		$V_I = V_{GS} = 2.5V$, $I = 200\text{mA}$		400		
P-Channel Leakage Current		$V_{DS} = 5.5V$			1	μA
N-Channel MOSFET On-Resistance		$V_I = V_{GS} = 3.6V$, $I = 200\text{mA}$		280	480	m Ω
		$V_I = V_{GS} = 2.5V$, $I = 200\text{mA}$		320		
N-Channel Leakage Current		$V_{DS} = 5.5V$			1	μA
P-Channel Current Limit	I_{LIM}	ILIM = V_{IN}	1400	1600	2000	mA
		ILIM = GND	600	900	1200	
ILIM High Level Input Voltage	V_{IH}		1.5			V
ILIM Low Level Input Voltage	V_{IL}				0.4	V
ILIM Input Leakage Current	I_{LKG}	EN=GND or V_{IN}		0.01		μA
Power Good Threshold	V_{PG}	Feedback voltage falling	88% V_O	92% V_O	96% V_O	V
PG Output Low Voltage	V_{OL}	$V_{FB} = 0.8 \times V_O$ nominal, $I_{SINK} = 10\mu\text{A}$			0.3	V
PG Output Leakage Current	I_{LKG}	$V_{FB} = V_O$ nominal		0.01		μA
Oscillator Frequency	f_S		1200	1500	1800	KHz
Synchronization Range	F_{SYNC}	CMOS-logic clock signal on SYNC pin	1000		2000	KHz
SYNC High Level Input Voltage	V_{IH}		1.5			V
SYNC Low Level Input Voltage	V_{IL}				0.4	V
SYNC Input Leakage Current	I_{LKG}	SYNC=GND or V_{IN}		0.01		μA
Duty Cycle of External Clock Signal			20		60	%
Reference Voltage	V_{REF}		0.436	0.45	0.464	V
Line Regulation		$V_{IN} = 2.5V$ to $5.5V$		0.05		% / V
Load Regulation		$V_{IN} = 5.5V$, $I_O = 10\text{mA}$ to 600mA		0.6		%
Start-up Time		$I_O = 0\text{mA}$, time from active EN to V_O		0.4		ms

Typical Performance Curves

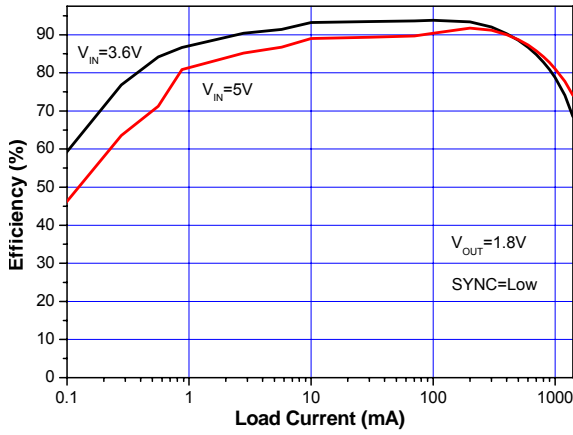


Figure 4. Efficiency vs. Load Current

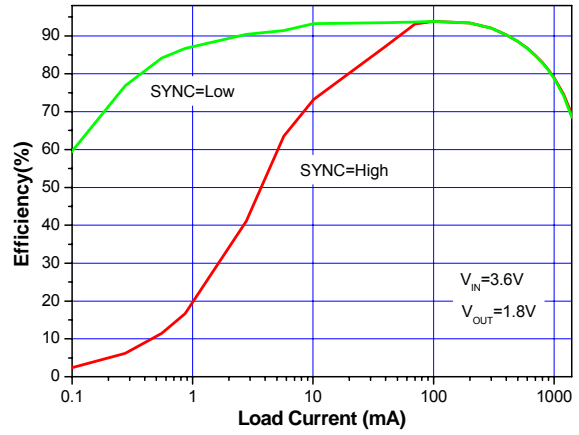


Figure 5. Efficiency vs. Load Current

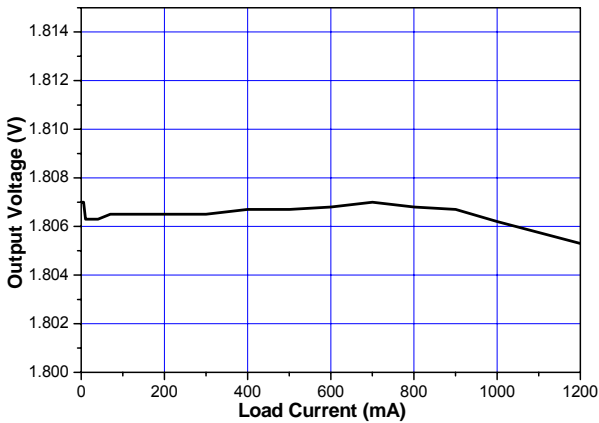


Figure 6. Output Voltage vs. Output Current (VIN=3.6V)

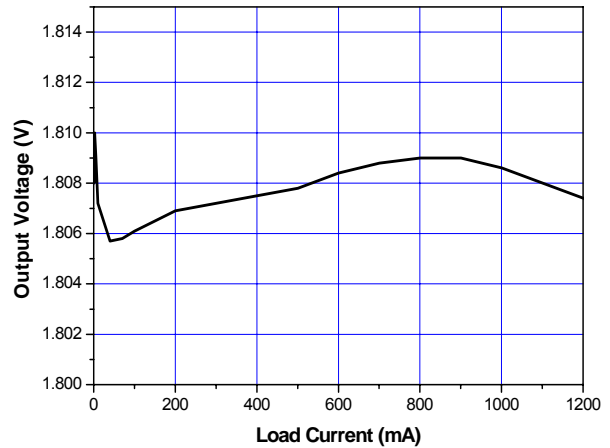


Figure 7. Output Voltage vs. Output Current (VIN=5V)

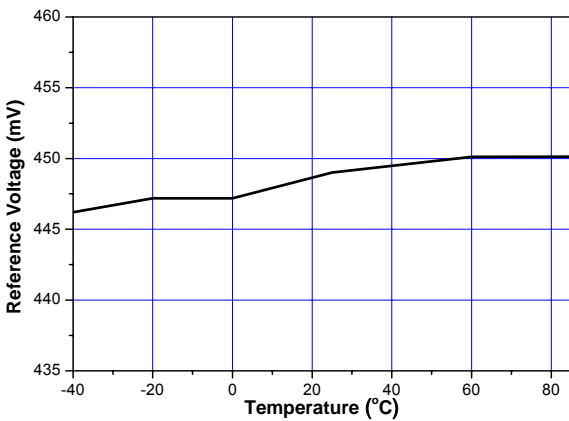


Figure 8. Reference Voltage vs. Junction Temperature

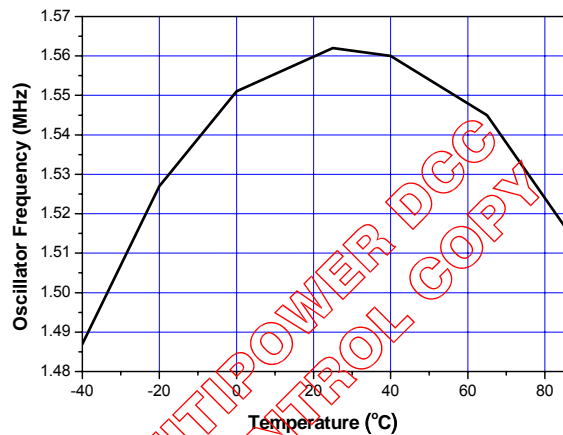


Figure 9. Frequency vs. Junction Temperature

Typical Performance Curves (Continued)

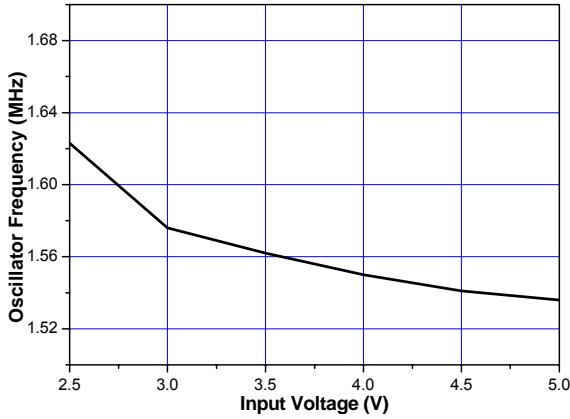


Figure 10. Frequency vs. Input Voltage

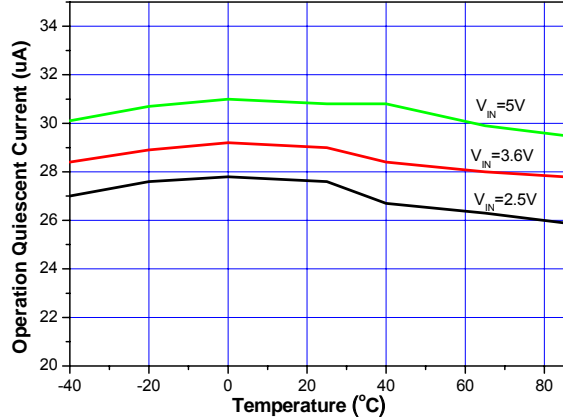


Figure 11. Quiescent Current vs. Junction Temperature

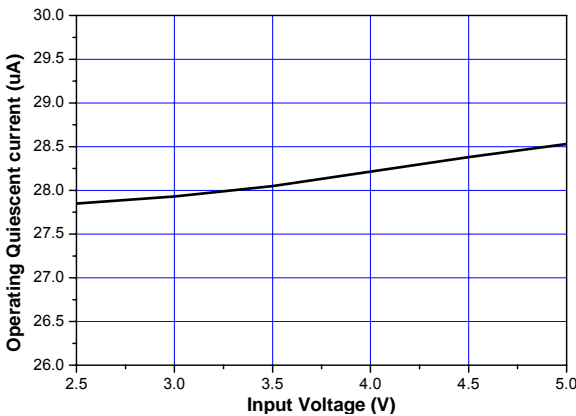


Figure 12. Quiescent Current vs. Input Voltage

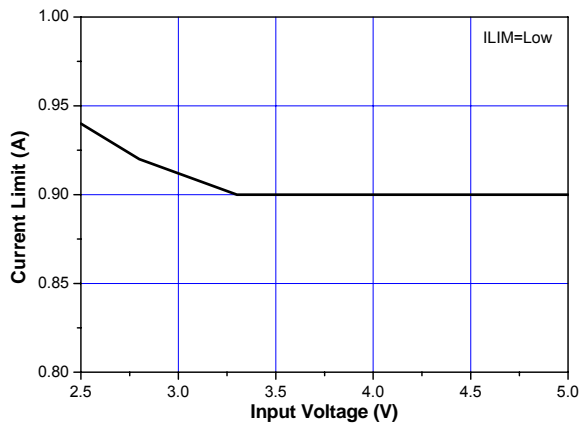


Figure 13. Current Limit vs. Input Voltage (ILIM=Low)

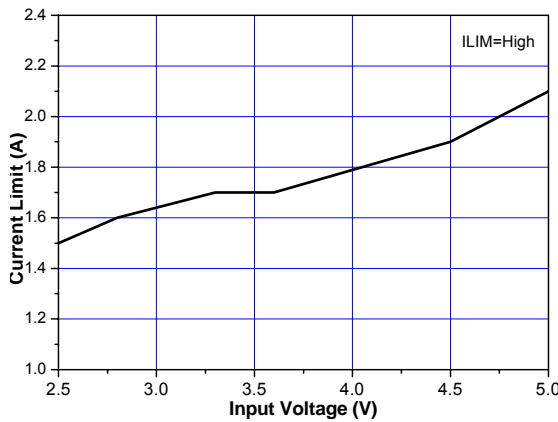


Figure 14. Current Limit vs. Input Voltage (ILIM =High)

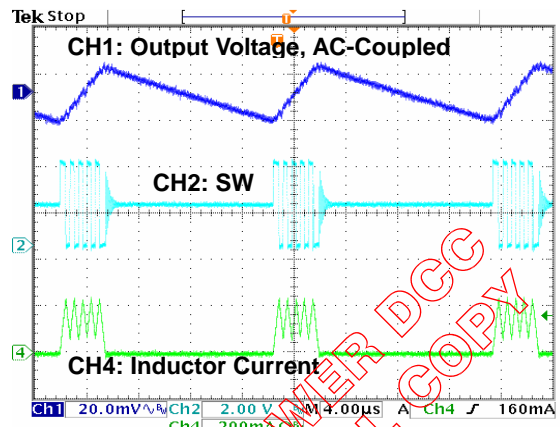
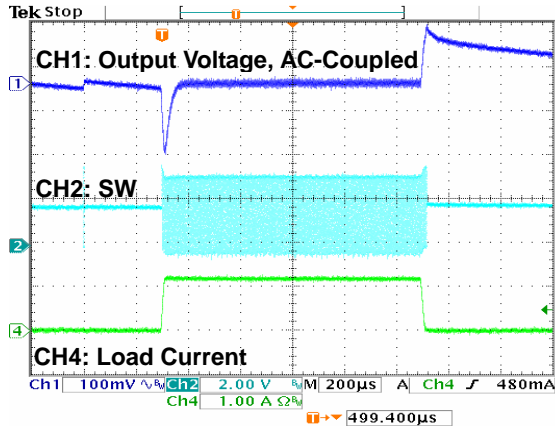


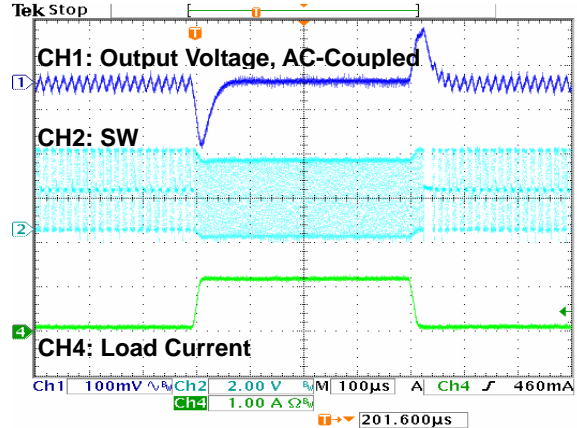
Figure 15. Light Load Waveform
 $V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=30mA$, $SYNC=Low$

Typical Performance Curves (Continued)



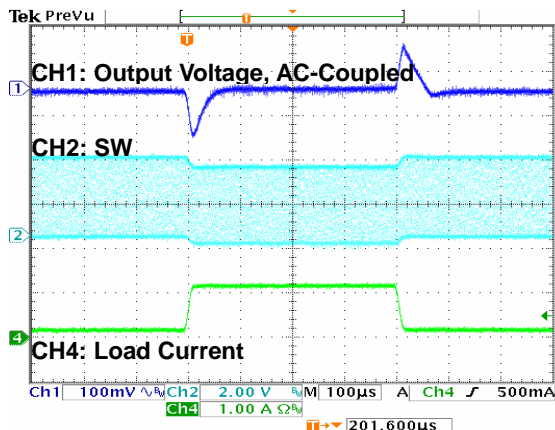
$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=1mA$ to 1.2A, SYNC=Low, ILIM=High

Figure 16. Load Transient Response



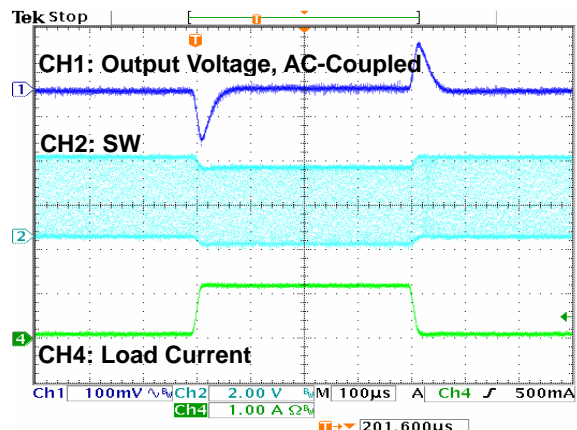
$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=100mA$ to 1.2A, SYNC=Low, ILIM=High

Figure 17. Load Transient Response



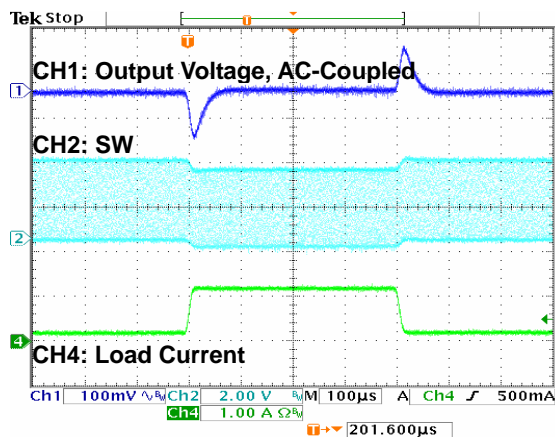
$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=200mA$ to 1.2A, SYNC=Low, ILIM=High

Figure 18. Load Transient Response



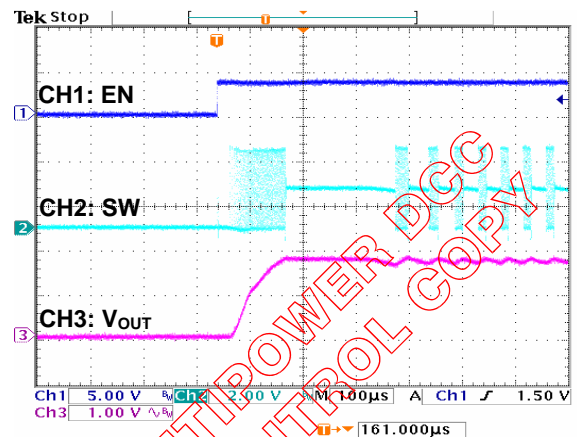
$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=100mA$ to 1.2A, SYNC=High, ILIM=High

Figure 19. Load transient Response



$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=200mA$ to 1.2A, SYNC=High, ILIM=High

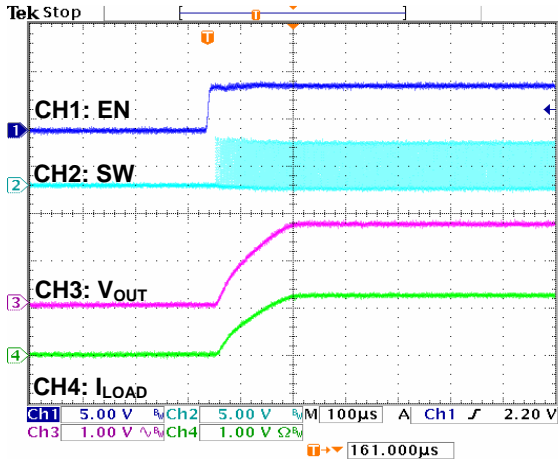
Figure 20. Load transient Response



$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $L=3.3\mu H$, $C_{OUT}=10\mu+0.1\mu$,
 $I_{LOAD}=30mA$, SYNC=Low, ILIM=High

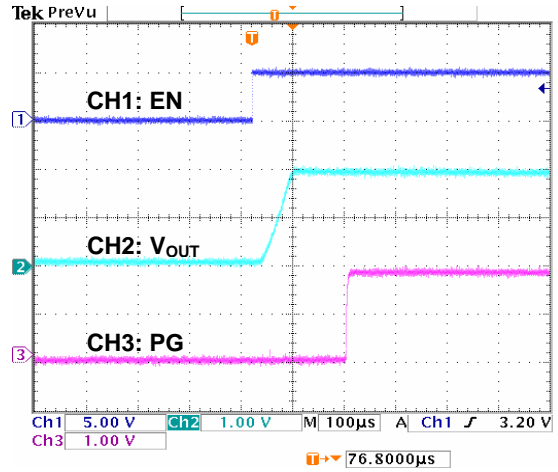
Figure 21. Light Load Start-up Waveform

Typical Performance Curves (Continued)



V_{IN}=3.6V, V_{OUT}=1.8V, L=3.3µH, C_{OUT}=10µ+0.1µ, I_{LOAD}=1.2A, SYNC=Low, ILIM=High

Figure 22. Heavy Load Start-up Waveform



V_{IN}=3.6V, V_{OUT}=1.8V, L=3.3µH, C_{OUT}=10µ+0.1µ, I_{LOAD}=0mA, SYNC=Low, ILIM=High

Figure 23. Power Good Waveform

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Application Information

Operation

The FP6365 is designed in a current mode PFM/PWM scheme which features an internal synchronous rectifier to eliminate an external schottky diode. The FP6365 operates in four modes to optimize performance. The forced PWM mode operates at a fixed 1.5MHz switching frequency. The synchronizable PWM mode allows an external clock to minimize harmonics. The PFM/PWM mode operates in PFM mode during light loads to maintain the highest efficiency to extend battery life and PWM mode under heavy load. The shutdown mode reduces quiescent current to 0.1uA.

As the input voltage approaches the output voltage, the maximum on-time can exceed one internal oscillator cycle, which allows operation up to 100% duty cycle. In 100% duty cycle operation, the output voltage is equal to the input voltage minus the voltage drop across the P-channel MOSFET.

The control loop is internally compensated reducing the amount of external components.

Forced PWM Mode and Power Saving Mode

Connect the SYNC to the VIN forces the converter to the PWM mode even at light or no load currents. The advantage is the converter operates with a fixed switching frequency that allows for noise sensitive applications. In this mode, the efficiency is lower than the power saving mode during light loads.

Connect the SYNC to the GND pin enables the power saving mode. The converter operates in the PWM mode at heavy loads and in the PFM mode during light loads improving efficiency over wide load current range. The output ripple is bigger during PFM operation. A larger output capacitor can be used to minimize ripple.

Synchronous Frequency Control

The internal oscillator of FP6365 is set for a fixed 1.5MHz switching frequency or can be synchronized to an external clock within a frequency range from 1MHz to 2MHz. The converter automatically detects the rising edge of the first clock and is synchronized immediately to the external clock. When the SYNC is clocked by an external signal, the device stays in forced PWM mode. If the clock signal is stopped, the converter switches to the internal clock automatically and without interruption. Do not leave SYNC unconnected.

Selectable Current Limit

The switch current is sensed internally. The current sense comparator monitors the high side P-channel MOSFET to detect over-current. This protects the system, internal MOSFETs and components eliminate overload conditions. Connecting ILIM to ground to set current limit in typical 0.9A or ILIM to Vin for 1.6A current limit.

Power Good Comparator

The power good (PG) comparator is an open drain output. The PG pin becomes active high when the output voltage exceeds 96% of its nominal value. The PG is high impedance when the FP6365 is disabled (EN = low) and active when the FP6365 is enabled (EN = high). Leave the PG pin floating if not used.

The PG output is not valid for the first 300µs after EN goes high as figure 22 shown. If the PG pin is connected to an external power source with a pull up resistor which might cause a spike. The false high signal have to be taken within the first 300µs after the device enable. To avoid false PG signals during start-up, a small R-C filter can be used to filter the spike.

Under Voltage Lockout

The under voltage lockout (UVLO) circuit provides the save operation to keeps the device from turning on when Vin is smaller than typically 1.65V.

Adjustable Output Voltage

The output voltage of FP6365 ranges from 0.8V to VIN which is set by the external feedback resistor. It can be calculated as:

$$V_{out} = 0.45 \times \left(1 + \frac{R1}{R2}\right)$$

Add a small feed forward capacitor (C_f) ranging from 22pF to 68pF in parallel with R1 for better stability, but the load transient response will degrade.

Application Information (Continued)

Inductor Selection

A 10uH is recommended for general used. The value of inductor depends on the operating frequency. Higher frequency allows smaller inductor and capacitor but increase internal switching loss. Two inductor parameters should be considered, current rating and DCR. The DCR of inductor affects the efficiency of the converter. The inductor with lowest DCR is chosen for highest efficiency.

The inductor value can be calculated as:

$$L = \frac{V_{OUT}}{f * \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

ΔI_L : inductor ripple current, which defined as:

$$\Delta I_L = V_o \left[1 - \frac{V_o}{V_i}\right] / (L * f)$$

The inductor should be rated for the maximum output current ($I_{O(MAX)}$) plus the inductor ripple current (ΔI_L) to avoid saturation. The maximum inductor current ($I_{L(MAX)}$) is given by:

$$I_{L(MAX)} = I_{O(max)} + \frac{\Delta I_L}{2}$$

Capacitor Selection

The FP6365 is permissible in using ceramic capacitor for hand held instruments application. The value of capacitor depends on acceptable voltage ripple.

The input capacitor can reduced peak current and noise at power source. It should have 10uF at least and can be increased for better input voltage filtering. Select the input capacitor to meet the input ripple current and voltage rating.

When selecting an output capacitor, consider the output ripple voltage and the ripple current. The ESR of capacitor is a major factor to the output ripple. For best performance, a low ESR output capacitor is required. The ripple voltage is given by:

$$\Delta V_o = \Delta I_L \left(ESR + \frac{1}{8 * f * C_o}\right)$$

The common aluminum-electrolytic capacitors have high ESR and should be avoided. Low ESR aluminum-electrolytic and tantalum capacitors are acceptable. Remember that do not exceed the ripple current ratings of tantalum capacitors. Ceramic capacitors have the lowest ESR in general, and OS-CON capacitors have the lowest ESR of the high value electrolytic types. When using very low ESR capacitors, such as ceramic or OS-CON, check for stability while consider load-transient response. It uses 10uF ceramic output capacitors for the FP6365 generally.

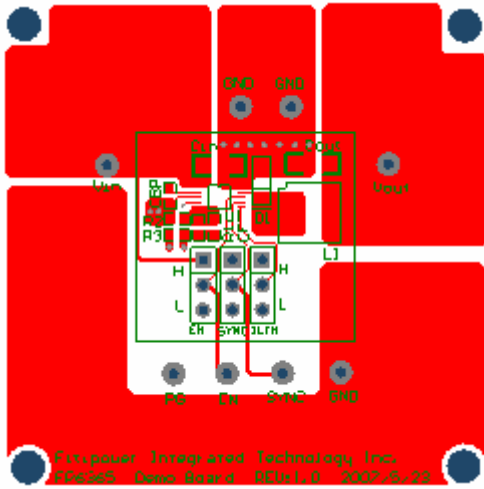
Layout Consideration

Figure 23 and 24 show the proper layout for the FP6365. Board layout is critical for all switch mode power supplies. The noise-sensitive feedback circuitry is isolated from the high-frequency switching nodes. The careful attention should be taken to the high-frequency, high current loops. Here are some suggestions to the layout of FP6365 design.

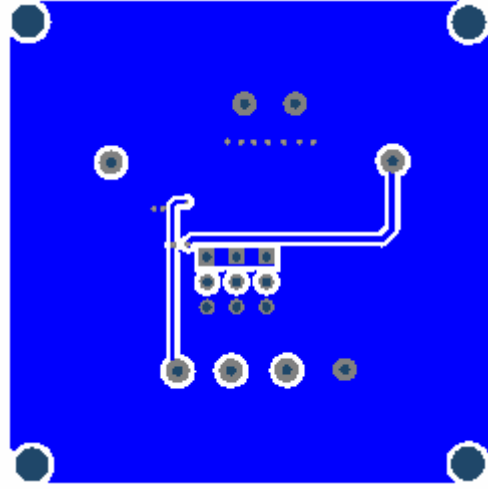
1. The input capacitor should be located as closed as possible to the VIN and PGND pin via wide route.
2. For best performance, minimize the high current and power ground loop are needed (SW→L1→Cout→PGND). The external components, Cout and L1, should be placed as close to the device as possible with short and wide route.
3. Keep feedback resistors, R1 and R2, near FB and GND pin with short wire and should be far away to the noise source, such as switching loop.
4. The GND and PGND pin can not connect directly. They should be isolated as much as possible, using via connection between them to minimize the effect of ground noise.

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Board Layout



Top Layer

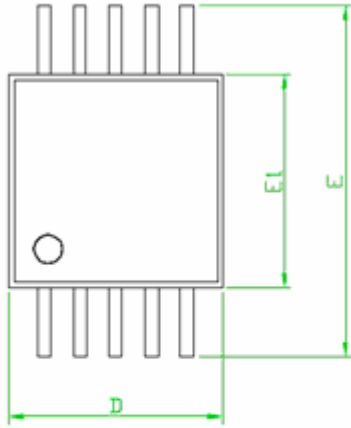


Bottom Layer

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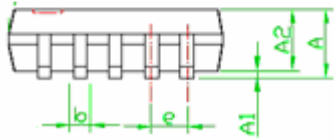
Outline Information

MSOP-10 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.10
A1	0.05	---	0.15
A2	0.75	0.85	0.95
b	0.17	---	0.33
C	0.08	0.15	0.23
D	---	3.00	---
E	---	4.90	---
E1	---	3.00	---
e	---	0.50	---
L	0.40	0.60	0.80
θ	0°	---	8°

Note 1: Followed From JEDEC MO-187-E.



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Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.