

Microprocessor Reset Circuits with Short Delay Time

Description

The FP6808 is a cost-effective system supervisor circuit designed to monitor microprocessor voltage and V_{DD} in digital systems. This device provides a reset signal to the host processor when necessary.

The circuit asserts a reset signal whenever the V_{DD} supply voltage declines below a preset threshold. It keeps reset signal asserted for at least 20ms after V_{DD} has risen above the reset threshold.

The FP6808-N has an open-drain active-low output stage, while FP6808-C has a push-pull active-low output. The FP6808-N's open-drain output requires a pull-up resistor.

The FP6808 is optimized to reject fast transient glitches on the V_{DD} line. Low supply current makes this device suitable for portable equipment.

Features

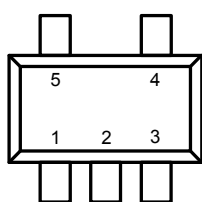
- Precision V_{DD} Monitor for 2.5V, 3.0V, 3.3V, and 5.0V Supplies.
- Precision Monitoring Voltages from 1.6V to 5.0V Available in 100mV Steps.
- 20 msec Guaranteed Minimum Reset Output Duration
- Low Supply Current
- $\pm 2\%$ High Precision Detection Voltage
- V_{DD} Transient Immunity
- Small SOT-23-5 Package
- No External Components
- Guaranteed Reset Valid to $V_{DD}=1V$
- Available in Two Output Configurations
 - Open-Drain Output (FP6808-N)
 - Push-Pull Output (FP6808-C)
- RoHS Compliant

Applications

- Computers
- Battery Powered Equipment
- Microprocessor Power Supply Monitoring
- Controllers
- Embedded Systems
- Automotive

Pin Assignments

S5 Package (SOT-23-5)



TOP VIEW

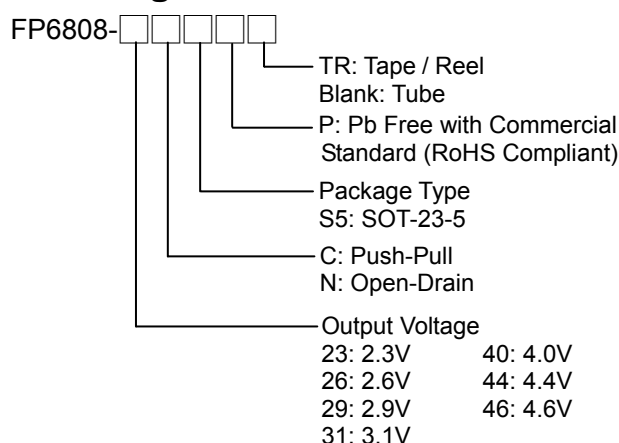
1. OUT
2. VDD
3. VSS
4. NC
5. NC

Figure 1. Pin Assignment of FP6808

SOT-23-5 Marking

Part Number	Product Code	Part Number	Product Code
FP6808-23NS5P	Ca	FP6808-23CS5P	Ck
FP6808-26NS5P	Cb	FP6808-26CS5P	Cm
FP6808-29NS5P	Cd	FP6808-29CS5P	Cn
FP6808-31NS5P	Ce	FP6808-31CS5P	Cr
FP6808-40NS5P	Cf	FP6808-40CS5P	Cs
FP6808-44NS5P	Ch	FP6808-44CS5P	Ct
FP6808-46NS5P	Ci	FP6808-46CS5P	Cu

Ordering Information



Typical Application Circuit

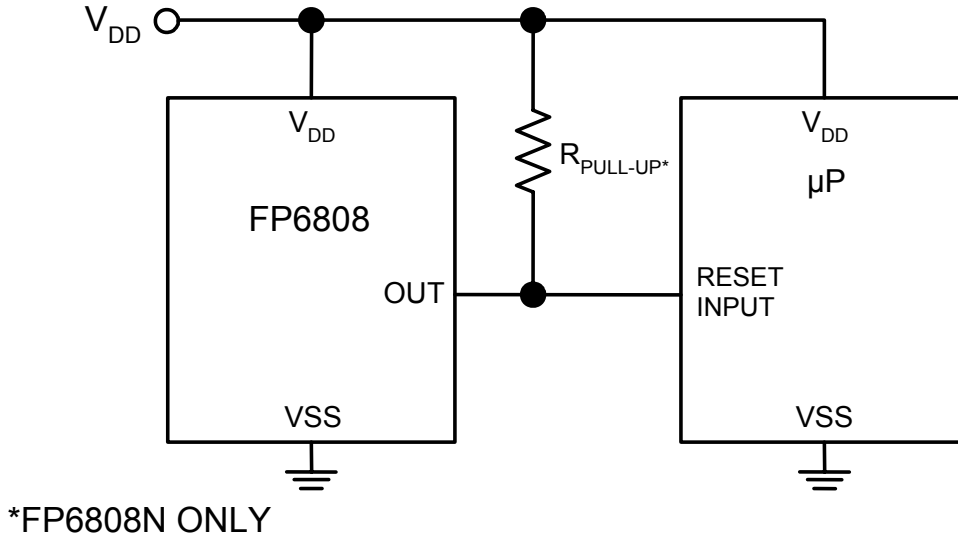


Figure 2. Typical Application Circuit of FP6808

Functional Pin Description

Pin Name	Pin Function
OUT	Voltage detection output pin
VDD	Voltage input pin
VSS	GND pin
NC ^{*1}	No connection

Note : *1. The NC pin is electrically open. The NC pin can be connected to VDD or VSS

Block Diagram

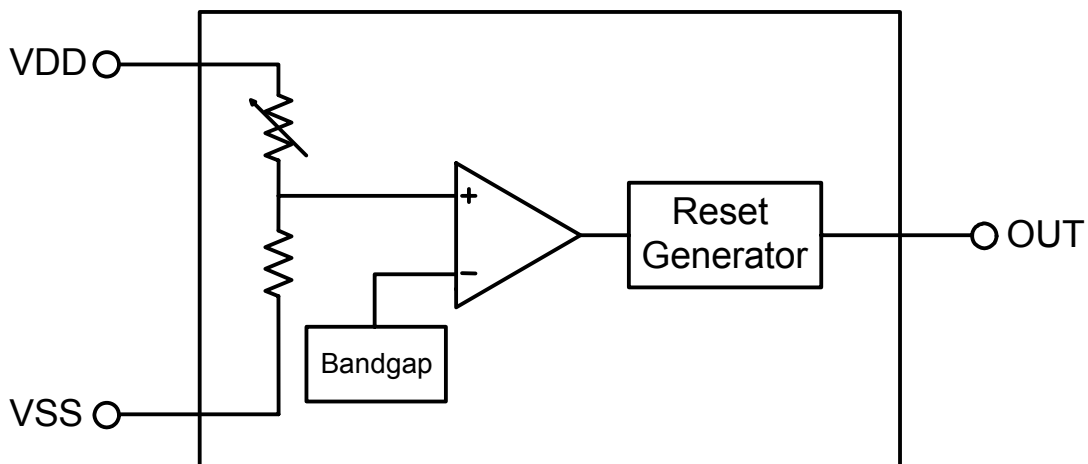


Figure 3. Block Diagram of FP6808

Absolute Maximum Ratings

- Supply Voltage (V_{DD} to V_{SS})----- -0.3V to +6V
- Output Voltage (Push-Pull)----- -0.3 to ($V_{DD}+0.3V$)
- Output Voltage (Open Drain)----- -0.3V to ($V_{DD}+0.3V$)
- Input Current (V_{DD}) ----- 20mA
- Output Current (I_{OUT})----- 20mA
- Rate of Rise (V_{DD})----- 100V/us
- Continuous Power Dissipation ($T_A=+70^{\circ}C$) :
 - 5-Pin SOT-23-5 (derate 4mW / $^{\circ}C$ above $+70^{\circ}C$)----- 320mW
- Operating Temperature Range (T_A)----- $-40^{\circ}C$ to $+105^{\circ}C$
- Storage Temperature (T_S)----- $-65^{\circ}C$ to $+150^{\circ}C$
- Lead Temperature (Soldering, 10s)----- $+300^{\circ}C$

Note : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{DD} to V_{SS})----- $+1.0V$ to $+5.5V$
- Operation Temperature Range----- $-40^{\circ}C$ to $+85^{\circ}C$

Electrical Characteristics

(V_{DD} =full range, $T_A=25^{\circ}C$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
V_{DD} Range	V_{DD}		1.0		5.5	μA
Supply Current	I_{DD}	$V_{DD} < 5.5V$, FP6808-46/44/40		3		μA
		$V_{DD} < 3.6V$, FP6808-23/26/29/31		3		
Reset Threshold	V_{TH}	FP6808-46	4.54	4.63	4.72	V
		FP6808-44	4.29	4.38	4.47	
		FP6808-40	3.92	4.00	4.08	
		FP6808-31	3.02	3.08	3.14	
Reset Threshold	V_{TH}	FP6808-29	2.87	2.93	2.99	V
		FP6808-26	2.58	2.63	2.68	
		FP6808-23	2.27	2.32	2.37	
Reset Threshold Tempco			30		ppm/ $^{\circ}C$	
V_{DD} to Reset Delay		$V_{DD} = V_{TH}$ to ($V_{th}-100mV$)		20		us
Reset Active Timeout Period			20	40	60	ms
Output Voltage Low (Push-Pull and Open-Drain)	V_{OL}	$V_{DD} = V_{TH}$ min, $I_{SINK}=1.2mA$, FP6808-23/26/29/31			0.3	V
		$V_{DD} = V_{TH}$ min, $I_{SINK}=3.2mA$, FP6808-44/46			0.4	
		$V_{DD} > 1.0V$, $I_{SINK}=50\mu A$			0.3	

Electrical Characteristics (Continued)

(V_{DD} =full range, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output Voltage High (push-pull)	V _{OH}	V _{DD} > V _{TH} max, I _{SOURCE} =500uA, FP6808-23/26/29/31	0.8 V _{DD}			
		V _{DD} > V _{TH} max, I _{SOURCE} =800uA, FP6808-44/46	V _{DD} -1.5			
Output Open-Drain Output Leakage Current (FP6808-N)		V _{DD} > V _{TH} , RESET deasserted			1	uA

Typical Performance Curves

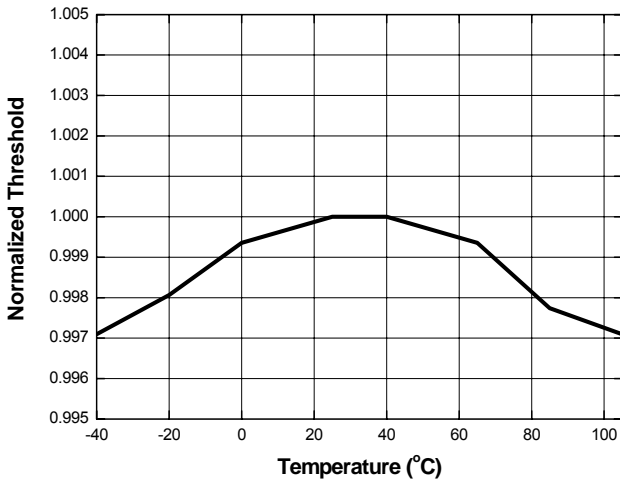


Figure 4. Normalized Reset Threshold vs. Temperature

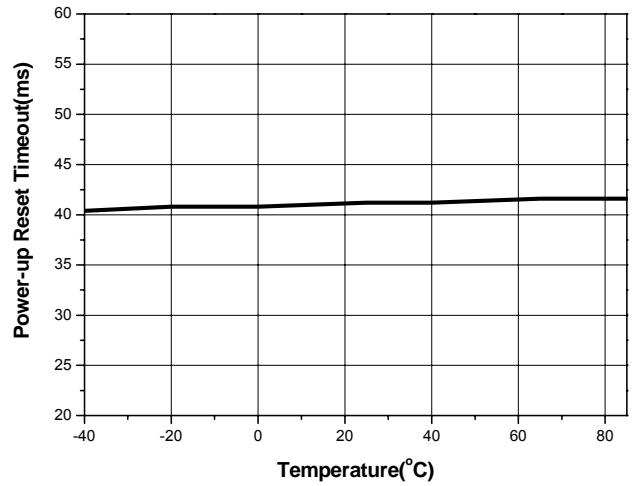


Figure 5. Power-up Timeout vs. Temperature

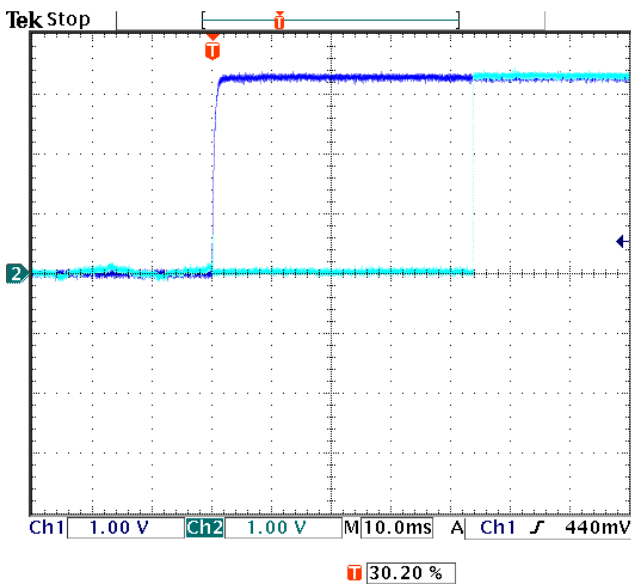


Figure 6. Power-Up $\overline{\text{RESET}}$ Timeout Waveforms; Ch1 : VDD Ch2 : OUT

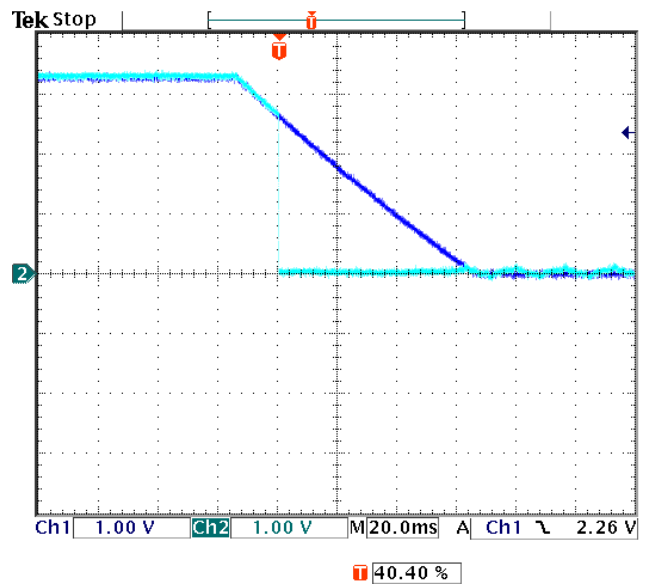


Figure 7. Power-Down $\overline{\text{RESET}}$ Delay Waveforms; Ch1 : VDD Ch2 : OUT

Typical Performance Curves (Continued)

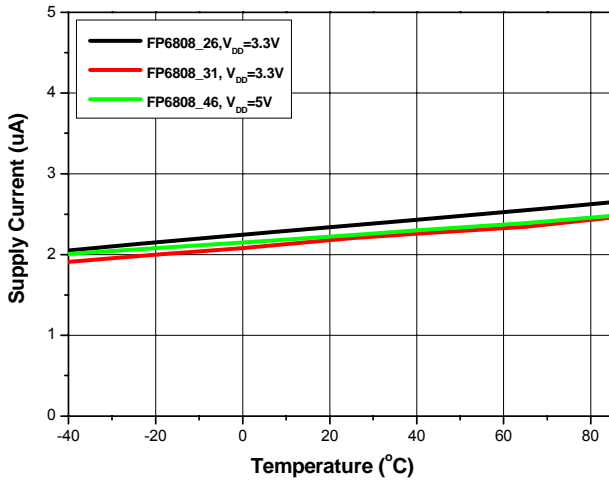


Figure 8. Supply Current vs. Temperature

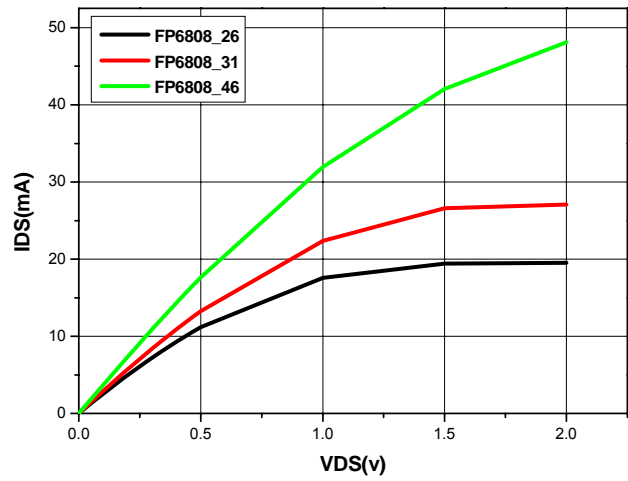


Figure 9. Output Sinking Capability

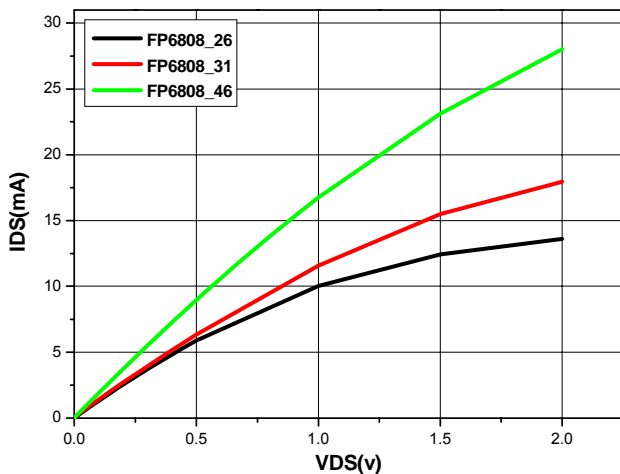


Figure 10. Output Sourcing Capability

Functional Description

FP6808 is supervisory circuit, monitoring critical voltages and asserting reset signal to the subsequent devices. The reset signal can start the micro-processor in a known state, avoiding code-execution errors during power-up, power-down, or brownout conditions. OUT is guaranteed to be a logic low for $V_{TH} > V_{CC} > 0.9V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps OUT low for the reset timeout. After this period, OUT goes high. If V_{CC} falls below the reset threshold, OUT goes low immediately.

Whenever V_{CC} drops below V_{TH} , the internal timer resets to zero and OUT goes low. The internal timer keeps activated only when $V_{CC} > V_{TH}$, and OUT remains low for the reset timeout interval.

Application Information

1. Benefits of Highly Accurate Reset Threshold

Most microprocessor supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when supply is 10% below nominal. In other words, the reset is guaranteed to assert after the power supply falls out of regulation, but keeps inactive even when power is at the minimum specified operating voltage of the system ICs.

2. Negative-Going V_{DD} Transients

In addition to issuing a reset to microprocessor during power-up, power-down, and brownout conditions, FP6808 is relatively immune to short-duration negative-going V_{CC} transients (glitches). Figure 11 shows typical transient duration vs. reset comparator overdrive, for which the FP6808 does not generate a reset signal. The graph was generated using a negative-going pulse applied to V_{DD} , as shown in Figure 12, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{DD} transient can have without causing a reset signal. As the reset comparator overdrive increases, the maximum allowable pulse width decreases. A typical 0.1 μ F bypass capacitor mounted as close as possible to the V_{DD} pin provides additional transient immunity.

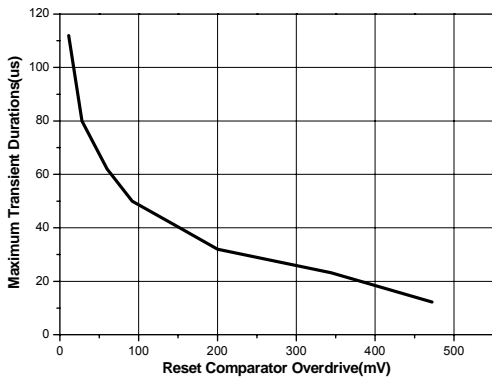


Figure 11. Maximum Transient Durations Without Causing a Reset Pulse vs. Reset Comparator Overdrive

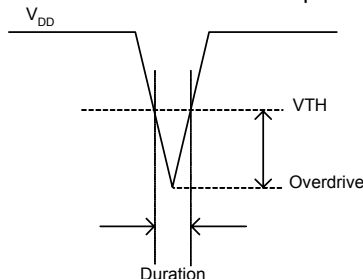


Figure 12. The V_{DD} with Negative Going Transients

3. Ensuring a Valid Reset Output Down to $V_{DD}=0$

When V_{DD} falls below 1V, the FP6808 no longer sinks current, it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to OUT can drift to undetermined voltages. This presents no problem in most applications for microprocessor's inoperative condition with V_{DD} below 1V. However, in applications where OUT must be valid down to 0V, adding a pull-down resistor to OUT causes stray leakage currents to flow to ground, providing some impedance between OUT and ground (Figure 13). R1 is recommended around 100k Ω .

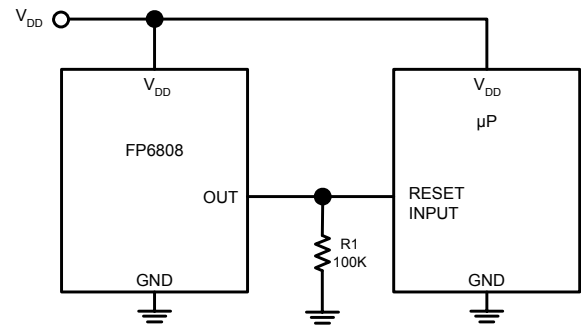


Figure 13. OUT Valid to $V_{DD}=\text{Ground}$ Circuit

3. Interfacing to uPs with Bidirectional Reset Pins

Since the output of FP6808N is open drain, this device interfaces easily with microprocessor that has bidirectional reset pins. Connect the FP6808N's output directly to the microcontroller's RESET pin with a single pull-up resistor allows either device to assert reset (Figure 14).

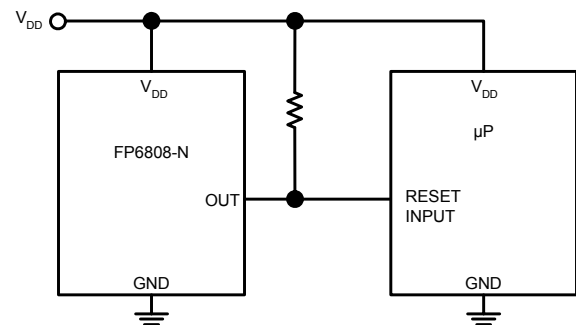
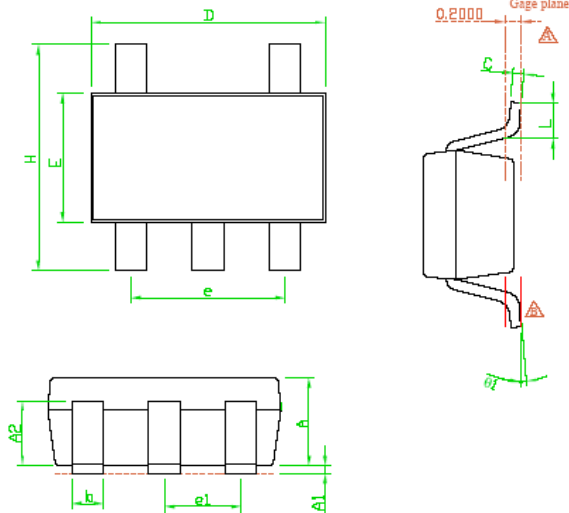


Figure 14. Interfacing to uPs with Bidirectional Reset I/O

Outline Information

SOT-23-5 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	---	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.50	1.60	1.80
e	---	1.90(TYP)	---
H	2.60	2.80	3.00
L	0.37	---	---
θ1	1°	5°	9°
e1	---	0.95(TYP)	---

Note 1 : Package Body Sizes Exclude Mold Flash Protrusions or Gate Burrs.

Note 2 : Tolerance ± 0.1000 mm(4mil) Unless Otherwise Specified.

Note 3 : Coplanarity : 0.1000 mm

Note 4 : Dimension L Is Measured in Gage plane.

Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.