

## 3-Pin Microprocessor Reset Circuits

### Description

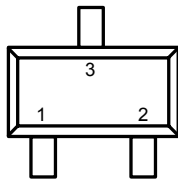
The FP6809 and FP6810 are cost-effective system supervisory circuits designed to monitor microprocessor voltage and  $V_{CC}$  in digital systems. They provide a reset signal to the host processor when necessary.

These circuits assert a reset signal whenever the  $V_{CC}$  supply voltage declines below a preset threshold. They keep reset signal asserted for at least 140ms after  $V_{CC}$  has risen above the reset threshold. The FP6809-N has an open-drain output stage, while FP6809-C and FP6810-C have push-pull outputs. The FP6809-N's open-drain output requires a pull-up resistor. The FP6809 has an active-low  $\overline{\text{RESET}}$  output while the FP6810 has an active-high RESET output.

The FP6809 and FP6810 are optimized to reject fast transient glitches on the  $V_{CC}$  line. Low supply current makes these devices suitable for portable equipments.

### Pin Assignments

#### S3 Package (SOT-23-3)



TOP VIEW  
 1. GND  
 2.  $\overline{\text{RESET}}$  (RESET)  
 3. VCC

Figure 1. Pin Assignment of FP6809/FP6810

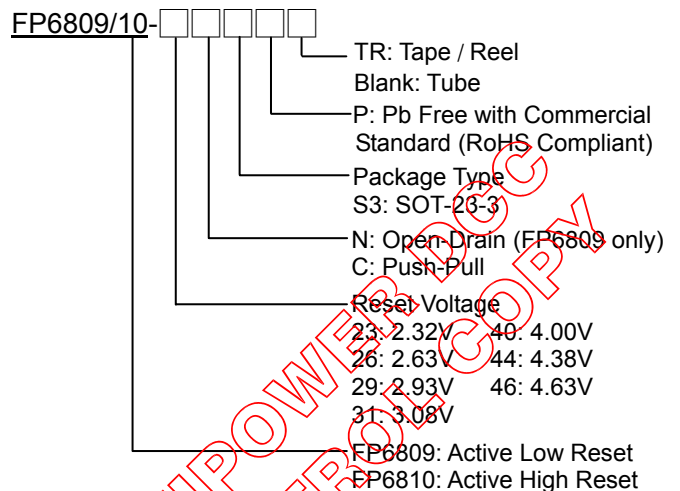
### Features

- Precision Monitoring of 2.5V, 3.0V, 3.3V, and 5.0V Power-Supply Voltages
- 140ms Guaranteed Minimum Reset Output Duration
- Low Supply Current
- $V_{CC}$  Transient Immunity
- Small SOT-23-3 Package
- No External Components
- Guaranteed Reset Valid to  $V_{CC}=1V$
- Available in Three Output Configurations
  - Open-Drain  $\overline{\text{RESET}}$  Output (FP6809-N)
  - Push-Pull  $\overline{\text{RESET}}$  Output (FP6809-C)
  - Push-Pull RESET Output (FP6810-C)
- RoHS Compliant

### Applications

- Computers
- Battery Powered Equipments
- Microprocessor Power Supply Monitoring
- Embedded Systems
- Automotive

### Ordering Information



Note : Please consult Fitipower sales office or authorized distributors for availability of special reset voltages.



SOT-23-3 Marking (FP6809)

| Part Number   | Product Code | Part Number   | Product Code |
|---------------|--------------|---------------|--------------|
| FP6809-23NS3P | Cv           | FP6809-23CS3P | CD           |
| FP6809-26NS3P | Cw           | FP6809-26CS3P | CE           |
| FP6809-29NS3P | Cx           | FP6809-29CS3P | CF           |
| FP6809-31NS3P | Cz           | FP6809-31CS3P | CG           |
| FP6809-40NS3P | CA           | FP6809-40CS3P | CH           |
| FP6809-44NS3P | CB           | FP6809-44CS3P | CJ           |
| FP6809-46NS3P | CC           | FP6809-46CS3P | CK           |

SOT-23-3 Marking (FP6810)

| Part Number   | Product Code | Part Number   | Product Code |
|---------------|--------------|---------------|--------------|
| FP6810-23CS3P | CL           | FP6810-40CS3P | CR           |
| FP6810-26CS3P | CM           | FP6810-44CS3P | CS           |
| FP6810-29CS3P | CN           | FP6810-46CS3P | CT           |
| FP6810-31CS3P | CP           |               |              |

Typical Application Circuit

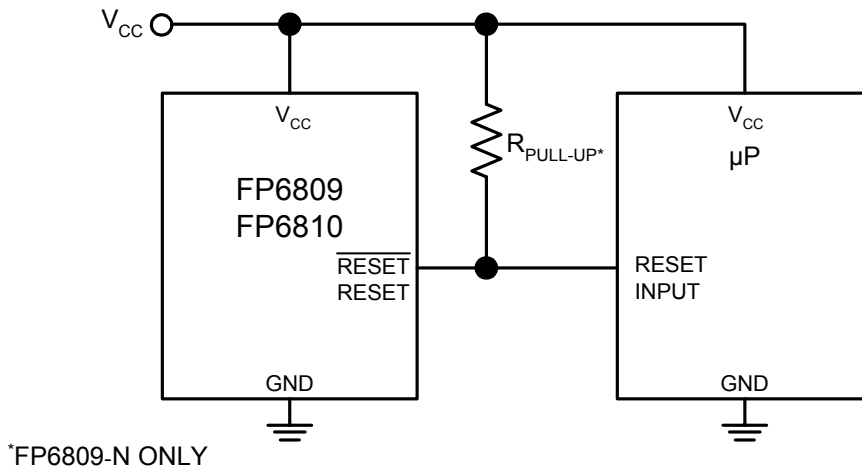


Figure 2. Typical Application Circuit of FP6809/FP6810

Functional Pin Description

| Pin Name                           | Pin Function   |
|------------------------------------|--|
| GND                                | Ground   |
| $\overline{\text{RESET}}$ (FP6809) | $\overline{\text{RESET}}$ Output remains low while $V_{CC}$ is below the reset threshold, and for at least 140ms after $V_{CC}$ rises above the reset threshold. |
| RESET (FP6810)                     | RESET Output remains high while $V_{CC}$ is below the reset threshold, and for at least 140ms after $V_{CC}$ rises above the reset threshold.                    |
| VCC                                | Supply Voltage   |

Block Diagram

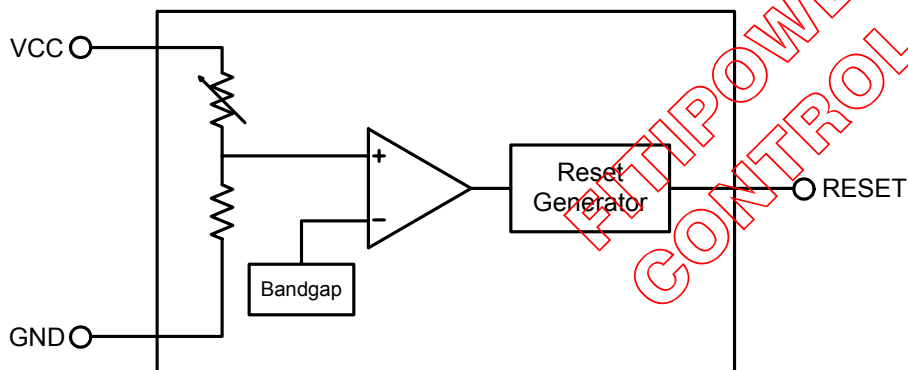


Figure 3. Block Diagram of FP6809/FP6810



## Absolute Maximum Ratings

- Supply Voltage ( $V_{CC}$  to GND) ----- -0.3V to +6V
- RESET,  $\overline{\text{RESET}}$  Voltage (Push-Pull)----- -0.3 to ( $V_{CC}+0.3V$ )
- $\overline{\text{RESET}}$  Voltage (Open Drain)----- -0.3V to ( $V_{CC}+0.3V$ )
- Input Current ( $V_{CC}$ ) ----- 20mA
- Output Current, RESET,  $\overline{\text{RESET}}$ ----- 20mA
- Rate of Rise ( $V_{CC}$ )----- 100V/us
- Continuous Power Dissipation ( $T_A=+70^\circ\text{C}$ ) :
  - 3-Pin SOT23 (derate 4mW/ $^\circ\text{C}$  above +70 $^\circ\text{C}$ )----- 320mW
- Operating Temperature Range ( $T_S$ )----- -40 $^\circ\text{C}$  to +105 $^\circ\text{C}$
- Storage Temperature ( $T_S$ )----- -65 $^\circ\text{C}$  to +150 $^\circ\text{C}$
- Lead Temperature (Soldering, 10s)----- +260 $^\circ\text{C}$

Note : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

## Recommended Operating Conditions

- Supply Voltage ( $V_{CC}$  to GND) ----- +1.0V to +5.5V
- Operation Temperature Range----- -40 $^\circ\text{C}$  to +85 $^\circ\text{C}$

## Electrical Characteristics

( $V_{CC}$ =full range,  $T_A=25^\circ\text{C}$ , unless otherwise specified.)

| Parameter   | Symbol   | Conditions  | Min  | Typ. | Max  | Unit                  |
|---|----------|---|------|------|------|-----------------------|
| $V_{CC}$ Range  | $V_{CC}$ |   | 1.0  |      | 5.5  | V                     |
| Supply Current  | $I_{CC}$ | $V_{CC}<5.5V$ , FP68__-46/44/40                                   |      | 3    |      | $\mu\text{A}$         |
|   |          | $V_{CC}<3.6V$ , FP68__-23/26/29/31                                |      | 3    |      |                       |
| Reset Threshold   | $V_{TH}$ | FP6809-46/ FP6810-46  | 4.54 | 4.63 | 4.72 | V                     |
|   |          | FP6809-44/ FP6810-44  | 4.29 | 4.38 | 4.47 |                       |
|   |          | FP6809-40/ FP6810-40  | 3.92 | 4.00 | 4.08 |                       |
|   |          | FP6809-31/ FP6810-31  | 3.02 | 3.08 | 3.14 |                       |
|   |          | FP6809-29/ FP6810-29  | 2.87 | 2.93 | 2.99 |                       |
|   |          | FP6809-26/ FP6810-26  | 2.58 | 2.63 | 2.68 |                       |
|   |          | FP6809-23/ FP6810-23  | 2.27 | 2.32 | 2.37 |                       |
| Reset Threshold Tempco  |          |   |      | 30   |      | ppm/ $^\circ\text{C}$ |
| $V_{CC}$ to Reset Delay   |          | $V_{CC}=V_{TH}$ to ( $V_{th}-100\text{mV}$ )                      |      | 20   |      | us                    |
| Reset Active Timeout Period   |          |   | 140  | 240  | 560  | ms                    |
| $\overline{\text{RESET}}$ Output Voltage Low (Push-Pull active low and Open-Drain active low, FP6809) | $V_{OL}$ | $V_{CC}=V_{TH}$ min, $I_{SINK}=1.2\text{mA}$ , FP6809-23/26/29/31 |      |      | 0.3  | V                     |
|   |          | $V_{CC}=V_{TH}$ min, $I_{SINK}=3.2\text{mA}$ , FP6809-44/46       |      |      | 0.4  |                       |
|   |          | $V_{CC}>1.0V$ , $I_{SINK}=50\mu\text{A}$                          |      |      | 0.3  |                       |

## Electrical Characteristics (Continued)

( $V_{CC}$ =full range,  $T_A=25^{\circ}\text{C}$ , unless otherwise specified.)

| Parameter   | Symbol   | Conditions   | Min     | Typ. | Max | Unit          |
|---|----------|--|---------|------|-----|---------------|
| RESET Output Voltage Low<br>(push-pull active high,<br>FP6810)                  | $V_{OL}$ | $V_{CC}=V_{TH}$ max, $I_{SINK}=1.2\text{mA}$ ,<br>FP6809-23/26/29/31     |         |      | 0.3 | V             |
|   |          | $V_{CC}=V_{TH}$ max, $I_{SINK}=3.2\text{mA}$ , FP6809-44/46              |         |      | 0.4 | V             |
| $\overline{\text{RESET}}$ Output Voltage High<br>(push-pull active low, FP6809) | $V_{OH}$ | $V_{CC}>V_{TH}$ max, $I_{SOURCE}=500\mu\text{A}$ ,<br>FP6809-23/26/29/31 | 0.8Vcc  |      |     | V             |
|   |          | $V_{CC}>V_{TH}$ max, $I_{SOURCE}=800\mu\text{A}$ , FP6809-44/46          | Vcc-1.5 |      |     | V             |
| RESET Output Voltage High<br>(push-pull active high,<br>FP6810)                 | $V_{OH}$ | $1.8\text{V}<V_{CC}<V_{TH}$ min, $I_{SOURCE}=150\mu\text{A}$             | 0.8Vcc  |      |     | V             |
| RESET Open-Drain Output<br>Leakage Current (FP6809-N)                           |          | $V_{CC}>V_{TH}$ , RESET deasserted                                       |         |      | 1   | $\mu\text{A}$ |

## Typical Performance Curves

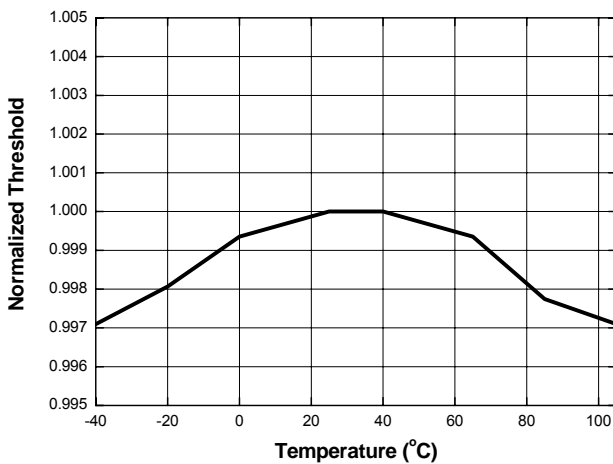


Figure 4. Normalized Reset Threshold vs. Temperature

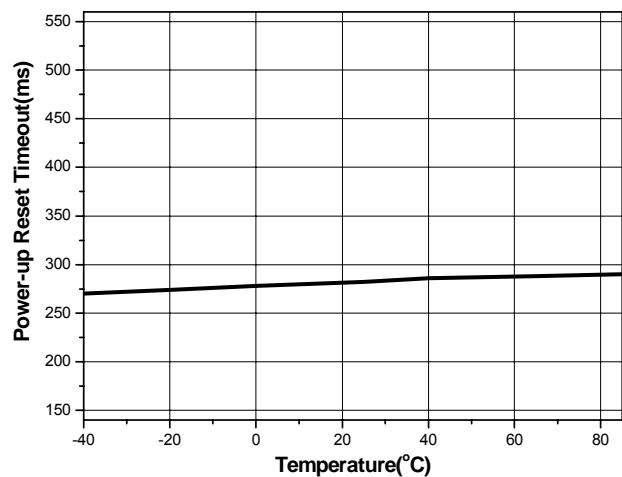


Figure 7. Power-up Timeout vs. Temperature

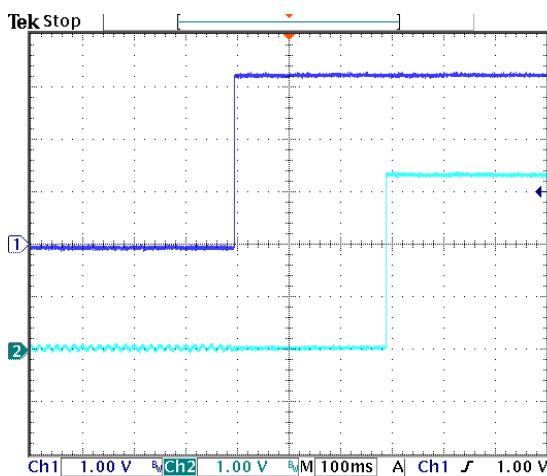


Figure 6. Power-Up  $\overline{\text{RESET}}$  Timeout Waveforms;  
Ch1 : VCC Ch2 :  $\overline{\text{RESET}}$

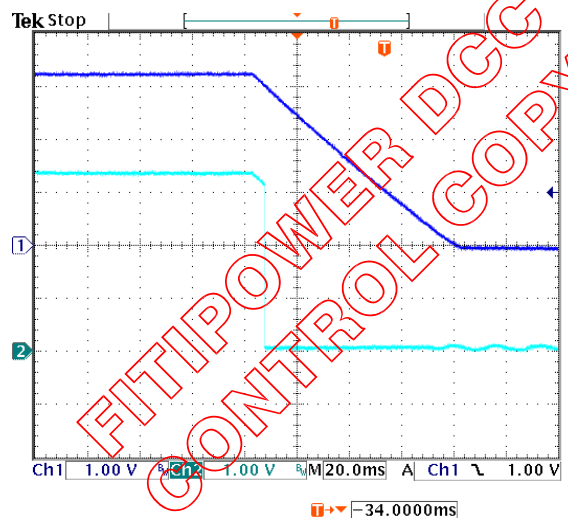


Figure 7. Power-Down  $\overline{\text{RESET}}$  Delay Waveforms;  
Ch1 : VCC Ch2 :  $\overline{\text{RESET}}$

## Typical Performance Curves (Continued)

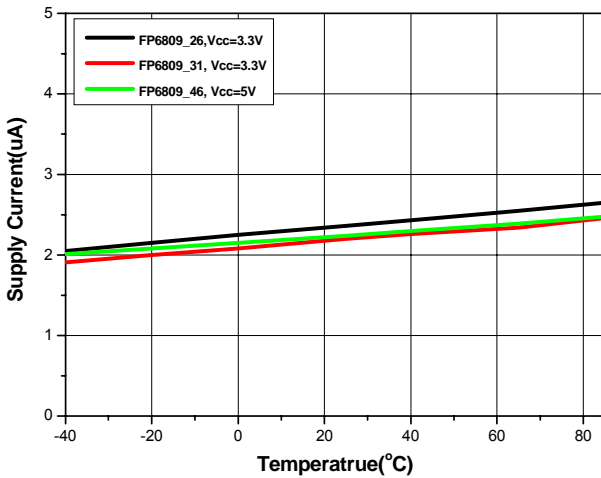


Figure 8. Supply Current vs. Temperature

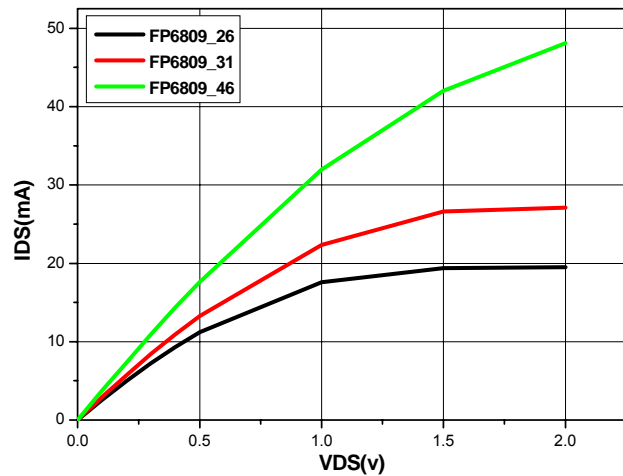


Figure 9. Output Sinking Capability

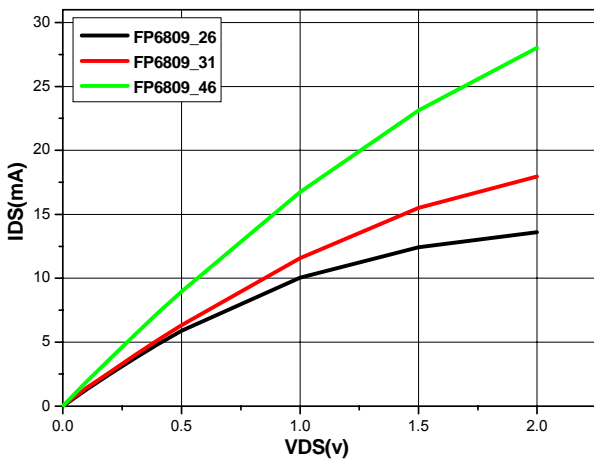


Figure 10. Output Sourcing Capability

## Functional Description

FP6809/FP6810 are supervisory circuits, monitoring critical voltages and asserting reset signal to the subsequent devices. The reset signal can start the microprocessor in a known state, avoiding code-execution errors during power-up, power-down, or brownout conditions.  $\overline{\text{RESET}}$ (RESET) is guaranteed to be a logic low (high) for  $V_{\text{TH}} > V_{\text{CC}} > 0.9\text{V}$ . Once  $V_{\text{CC}}$  exceeds the reset threshold, an internal timer keeps  $\overline{\text{RESET}}$ (RESET) low (high) for the reset timeout. After this period,  $\overline{\text{RESET}}$ (RESET) goes high (low). If  $V_{\text{CC}}$  falls below the reset threshold,  $\overline{\text{RESET}}$ (RESET) goes low (high) immediately.

Whenever  $V_{\text{CC}}$  drops below  $V_{\text{TH}}$ , the internal timer resets to zero and  $\overline{\text{RESET}}$ (RESET) goes low (high). The internal timer keeps activated only when  $V_{\text{CC}} > V_{\text{TH}}$ , and  $\overline{\text{RESET}}$ (RESET) remains low (high) for the reset timeout interval.

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## Application Information

### 1. Benefits of Highly Accurate Reset Threshold

Most microprocessor supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when supply is 10% below nominal. In other words, the reset is guaranteed to assert after the power supply falls out of regulation, but keeps inactive even when power is at the minimum specified operating voltage of the system ICs.

### 2. Negative-Going $V_{CC}$ Transients

In addition to issuing a reset to microprocessor during power-up, power-down, and brownout conditions, FP6809/FP6810 are relatively immune to short-duration negative-going  $V_{CC}$  transients (glitches). Figure 11 shows typical transient duration vs. reset comparator overdrive, for which the FP6809/FP6810 do not generate a reset signal. The graph was generated using a negative-going pulse applied to  $V_{CC}$ , as shown in Figure 12, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going  $V_{CC}$  transient can have without causing a reset signal. As the reset comparator overdrive increases, the maximum allowable pulse width decreases. A typical 0.1uF bypass capacitor mounted as close as possible to the  $V_{CC}$  pin provides additional transient immunity.

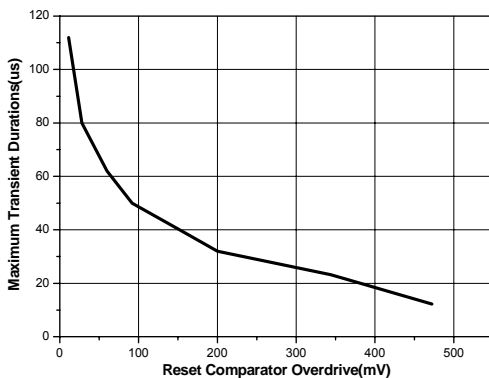


Figure 11. Maximum Transient Durations Without Causing a Reset Pulse vs. Reset Comparator Overdrive

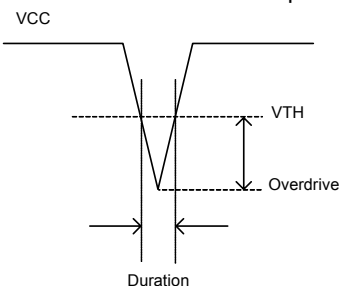


Figure 12. The  $V_{CC}$  with Negative Going Transients

### 3. Ensuring a Valid Reset Output Down to $V_{CC}=0$

When  $V_{CC}$  falls below 1V, the FP6809 no longer sinks current, it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications for microprocessor's inoperative condition with  $V_{CC}$  below 1V. However, in applications where RESET must be valid down to 0V, adding a pull-down resistor to RESET causes stray leakage currents to flow to ground, providing some impedance between RESET and ground (Figure 13). R1 is recommended around 100k $\Omega$ .

A 100k $\Omega$  pull-up resistor to  $V_{CC}$  is also recommended for FP6810 if RESET is required to remain valid for  $V_{CC}<1V$ .

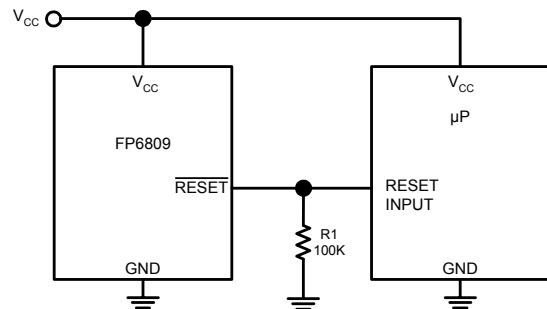


Figure 13.  $\overline{\text{RESET}}$  Valid to  $V_{CC}=\text{Ground}$  Circuit

### 3. Interfacing to uPs with Bidirectional Reset Pins

Since the RESET output of FP6809N is open drain, this device interfaces easily with microprocessor that has bidirectional reset pins. Connect the FP6809N's RESET output directly to the microcontroller's RESET pin with a single pull-up resistor allows either device to assert reset (Figure 14).

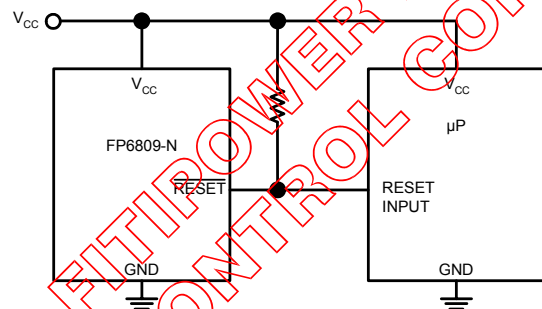
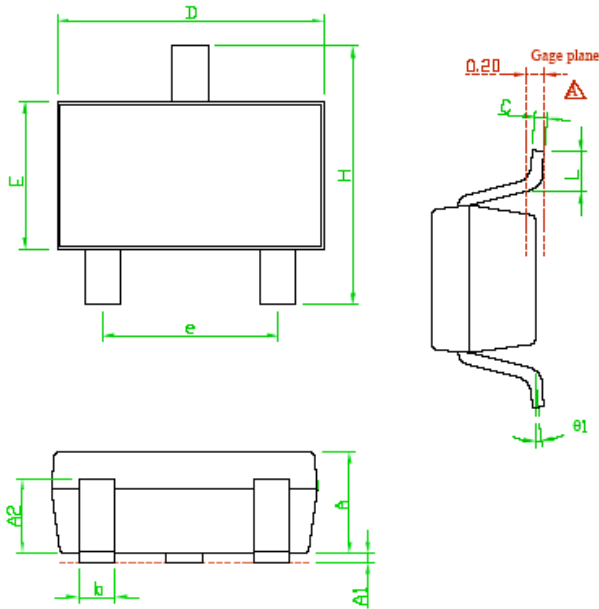


Figure 14. Interfacing to uPs with Bidirectional Reset I/O

**Outline Information**

**SOT-23-3 Package (Unit: mm)**



| SYMBOLS UNIT | DIMENSION IN MILLIMETER |           |      |
|--------------|-------------------------|-----------|------|
|              | MIN                     | NOM       | MAX  |
| A            | 1.00                    | 1.10      | 1.30 |
| A1           | 0.00                    | ---       | 0.10 |
| A2           | 0.70                    | 0.80      | 0.90 |
| b            | 0.35                    | 0.40      | 0.50 |
| C            | 0.10                    | 0.15      | 0.25 |
| D            | 2.70                    | 2.90      | 3.10 |
| E            | 1.40                    | 1.60      | 1.80 |
| e            | ---                     | 1.90(TYP) | ---  |
| H            | 2.60                    | 2.80      | 3.00 |
| L            | 0.37                    | ---       | ---  |
| θ1           | 1°                      | 5°        | 9°   |

- Note 1 : Package Body Sizes Exclude Mold Flash Protrusions or Gate Burrs.
- Note 2 : Tolerance ± 0.1000 mm(4mil) Unless Otherwise Specified.
- Note 3 : Coplanarity : 0.1000 mm
- Note 4 : Dimension L Is Measured in Gage plane.

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